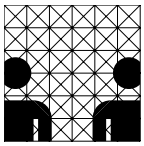
Benchmarkergebnisse



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Inhaltsverzeichnis

Hier sind die Ergebnisse der Benchmarks zur VHDL-Simulation in Form von Tabellen und Graphiken zusammengefasst. Da aus den Graphiken keine genauen Werte abgelesen werden können, enthält die Dissertation nur einige (aussagekräftige). Die dort präsentierten Ergebnisse lassen sich ohnehin besser anhand der Tabellen begründen.

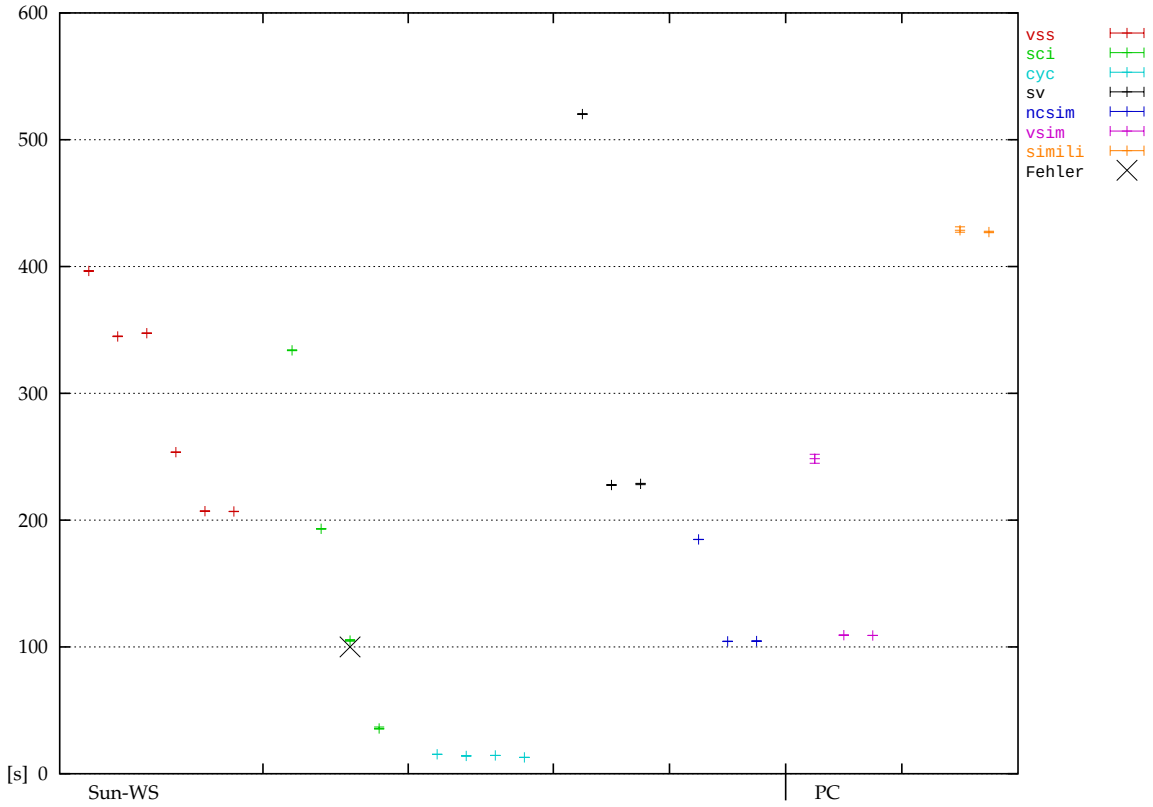
1 Operationswerk

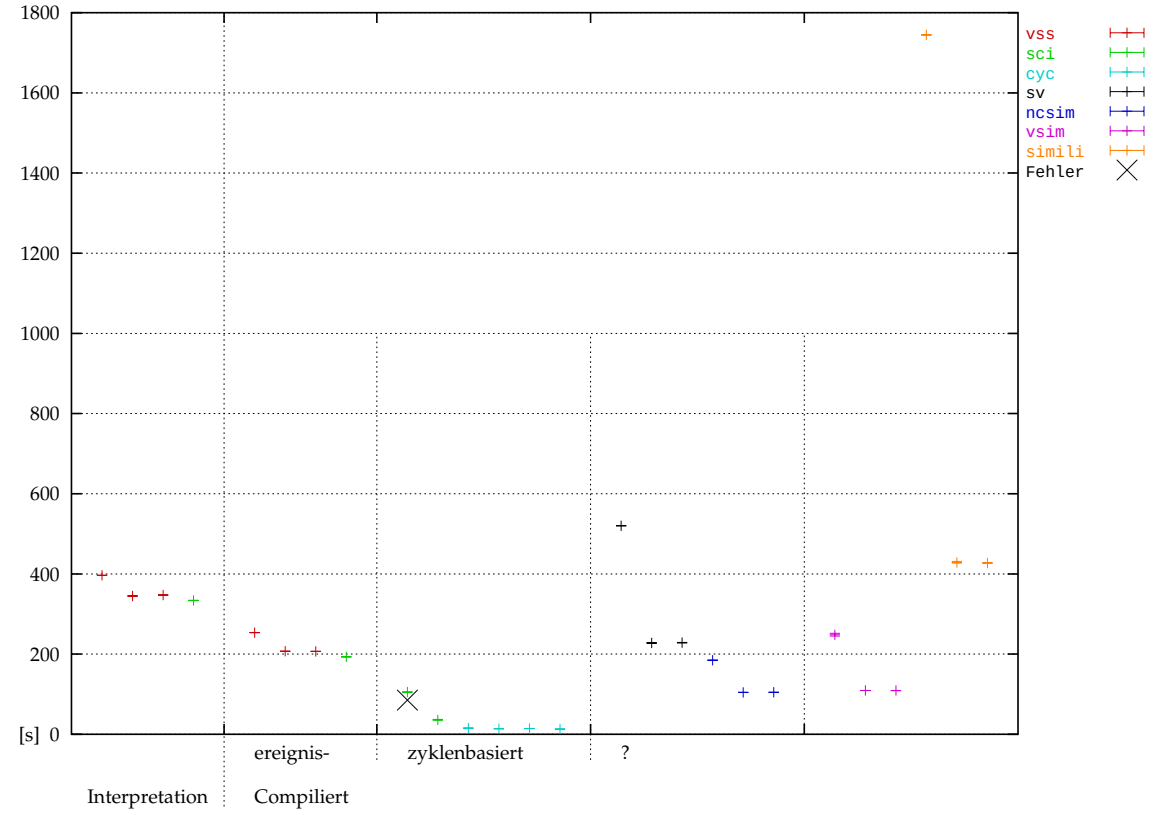
1.1 Register-Transfer Beschreibung

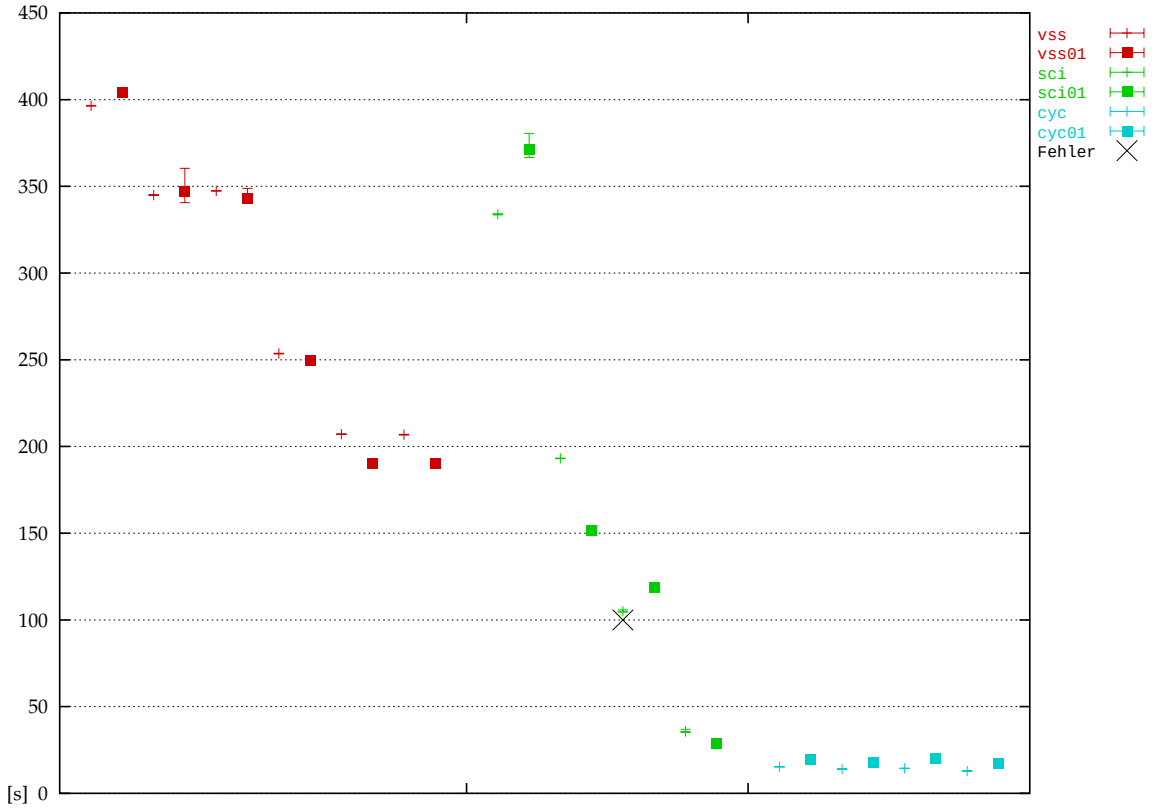
Tabelle 1: Operationswerk, RT-Code

Register-Transfer Code							
Simulator	avg. $[s]$	min.	max.	speed-up		Parameter	Fehler
VSS	396,52	396,31	396,64	0,52	0,52	vss.1	
	344,9	344,73	345,21	0,6	0,6	vss.2	
	347,4	347,36	347,47	0,6	0,6	vss.3	
	253,62	253,37	253,76	0,82	0,82	vss.4	
	207,07	206,98	207,23	1,0	1,0	vss.5	
	206,82	206,64	206,97	$*$	$*$	vss.6	
VSS '01	404,28	403,59	404,73	0,47	0,51	vss.1	
	347,24	340,59	360,38	0,55	0,6	vss.2	
	343,18	340,15	348,77	0,55	0,6	vss.3	
	249,69	248,87	250,45	0,76	0,83	vss.4	
	190,23	190,15	190,34	1,0	1,09	vss.5	
	190,11	189,85	190,46	$*$	1,09	vss.6	
Scirocco	333,9	333,58	334,23	0,11	0,62	sci.1	
	193,12	193,01	193,21	0,19	1,07	sci.2	
	104,99	104,51	105,81	0,34	1,97	sci.3	opw.1
	35,75	35,16	36,89	$*$	5,79	sci.4	
Scirocco '01	371,38	366,62	380,56	0,08	0,56	scs.1	
	151,5	151,32	151,6	0,19	1,37	scs.2	
	118,73	117,75	120,41	0,24	1,74	scs.3	
	28,77	28,73	28,82	$*$	7,19	scs.4	
Scirocco '02	319,33	318,13	321,57	0,08	0,65	scs.1	
	104,24	103,76	105,01	0,25	1,98	scs.2	
	67,01	66,89	67,22	0,38	3,09	scs.3	
	25,66	25,58	25,83	$*$	8,06	scs.4	
Cyclone	15,27	15,22	15,38	0,84	13,54	cyc.1	
	14,02	13,98	14,07	0,92	14,75	cyc.2	
	14,4	14,37	14,46	0,89	14,36	cyc.3	
	12,85	12,77	12,91	$*$	16,09	cyc.4	
Cyclone '01	19,44	19,4	19,53	0,89	10,64	cyc.1	
	17,53	17,48	17,57	0,98	11,78	cyc.2	
	20,29	20,1	20,48	0,85	10,19	cyc.3	
	17,24	17,15	17,3	$*$	12,0	cyc.4	
Leapfrog	520,27	520,16	520,37	0,44	0,4	lea.1	
	227,68	227,44	227,91	1,0	0,91	lea.2	
	228,63	227,93	229,05	$*$	0,9	lea.3	
NCSim	184,76	184,7	184,84	0,57	1,12	ncs.1	
	104,43	104,24	104,56	1,0	1,98	ncs.2	
	104,65	104,39	104,8	$*$	1,98	ncs.3	
ModelSim	248,4	244,81	251,99	0,44		mod.1	
	109,28	109,25	109,3	1,0		mod.2	
	109,08	109,02	109,14	$*$		mod.3	
Simili	1744,46	1743,62	1745,31	0,24		sim.1	
	428,59	427,03	431,26	1,0		sim.2	
	427,15	426,61	427,81	$*$		sim.3	

Operationswerk







1.2 RT-Beschreibung, Referenz zur Netzliste

Tabelle 2: Operationswerk, RT-Code, Referenz zur Netzliste

Register-Transfer Code						Referenzzyklen	
Simulator	avg. [s]	min.	max.	speed-up		Parameter	Fehler
VSS	19,77	19,75	19,8	0,48	77,77	vss.1	
	16,84	16,81	16,86	0,57	91,3	vss.2	
	17,1	16,94	17,37	0,56	89,91	vss.3	
	12,37	12,33	12,39	0,77	124,29	vss.4	
	9,52	9,5	9,53	1,0	161,5	vss.5	
	9,54	9,45	9,67	*	161,16	vss.6	
	20,04	20,0	20,09	0,48	76,72	vss.1 -gen	
	17,14	16,96	17,44	0,56	89,7	vss.2 -gen	
	17,17	16,92	17,54	0,56	89,54	vss.3 -gen	
	12,54	12,47	12,67	0,76	122,6	vss.4 -gen	
	9,83	9,62	10,22	0,97	156,4	vss.5 -gen	
	9,7	9,69	9,72	0,98	158,5	vss.6 -gen	
Scirocco	17,42	17,37	17,47	0,16	88,26	sci.1	
	10,67	10,39	11,18	0,26	144,09	sci.2	
	6,35	5,62	7,75	0,44	242,12	sci.3	opw.1
	34,88	34,05	36,51			sci.4	opw.2

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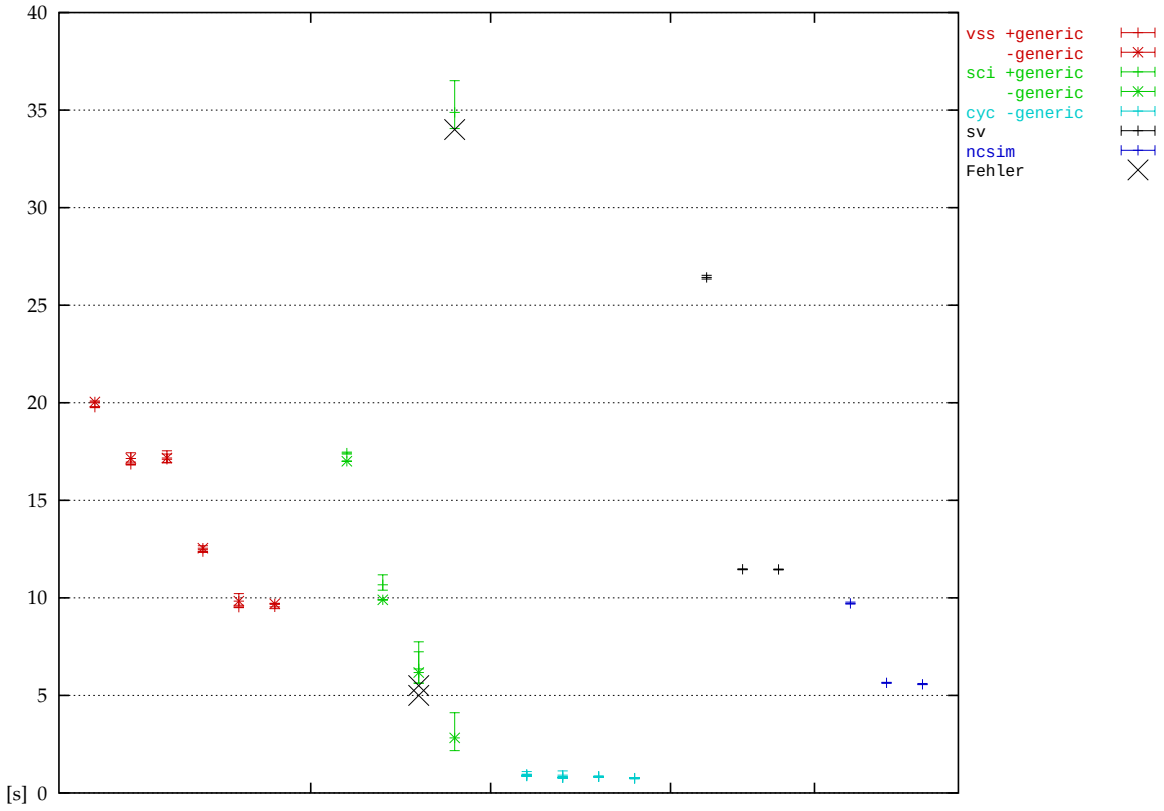
Register-Transfer Code						Referenzzyklen		
Simulator	avg. [s]	min.	max.	speed-up		Parameter		Fehler
	17,0	16,99	17,01	0,17	90,44	sci.1	-gen	
	9,9	9,9	9,9	0,28	155,3	sci.2	-gen	
	6,18	5,64	7,24	0,46	248,78	sci.3	-gen	opw.1
	2,82	2,17	4,11	∗	545,19	sci.4	-gen	
Scirocco '02	15,44	15,33	15,57	0,11	99,57	scs.1		
	5,5	5,41	5,63	0,31	279,53	scs.2		
	3,55	3,49	3,66	0,48	433,08	scs.3		opw.1
	1,71	1,67	1,79	∗	899,08	scs.4		
Cyclone	0,9	0,86	1,1	0,84	1708,26	cyc.1	-gen	
	0,82	0,76	1,13	0,93	1874,91	cyc.2	-gen	
	0,84	0,81	0,87	0,9	1830,27	cyc.3	-gen	
	0,76	0,73	0,78	∗	2022,93	cyc.4	-gen	
Leapfrog	26,42	26,34	26,53	0,43	58,19	lea.1		
	11,46	11,44	11,48	1,0	134,16	lea.2		
	11,45	11,43	11,47	∗	134,27	lea.3		
NCSim	9,72	9,68	9,78	0,57	158,17	ncs.1		
	5,65	5,62	5,67	0,99	272,11	ncs.2		
	5,57	5,55	5,61	∗	276,02	ncs.3		



1.3 Netzliste, VHDL Simulation

Tabelle 3: Operationswerk, AMS-Netzliste

Netzliste – VHDL						AMS-Prozess		
Simulator	avg. $[s]$	min.	max.	speed-up		Parameter		Fehler
VSS	803,16	801,54	804,45	1,91	1,91	vss.6	FTGS	
	827,56	825,02	829,26	1,86	1,86	vss.6	FTGSC	
	3194,62	3181,3	3204,33	0,48	0,48	vss.6	FTSM	
	333,4	333,16	333,76	4,61	4,61	vss.6	UDSM	opw.3
	2189,94	2189,49	2190,3	0,7	0,7	vss.6	VITAL	
	1537,43	1533,89	1542,3	$*$	$*$	vss.6	vital	
VSS ’01	808,14	805,06	813,73	1,94	1,9	vss.6	FTGS	
	801,25	798,04	806,87	1,96	1,92	vss.6	FTGSC	
	3182,39	3172,65	3197,21	0,49	0,48	vss.6	FTSM	
	339,8	333,99	345,7	4,62	4,52	vss.6	UDSM	opw.3
	2237,75	2215,45	2264,31	0,7	0,69	vss.6	VITAL	
	1570,26	1562,91	1574,24	$*$	0,98	vss.6	vital	
Scirocco ’01	1439,91	1391,01	1488,8	0,5	1,07	scs.2		
	744,24	739,85	748,62	0,97	2,07	scs.3		opw.1
	720,25	696,42	744,07	$*$	2,13	scs.4		opw.1
Scirocco ’02	1649,29	1630,55	1668,01	0,42	0,93	scs.2		
	741,47	737,56	745,37	0,94	2,07	scs.3		opw.1
	695,1	694,75	695,44	$*$	2,21	scs.4		opw.1
Leapfrog	211,03	210,43	211,84	0,7	7,29	lea.2		
	154,76	154,45	155,17	0,96	9,93	lea.3		
	148,37	148,14	148,75	1,0	10,36	lea.2	opt	
	148,27	148,07	148,43	$*$	10,37	lea.3	opt	
NCSim	317,33	315,2	320,08	0,25	4,84	ncs.2	vhdl	
	229,15	228,02	230,98	0,35	6,71	ncs.3	vhdl	
	98,31	97,54	99,2	0,81	15,64	ncs.2	vlog	
	79,38	79,33	79,47	$*$	19,37	ncs.3	vlog	

Operationswerk

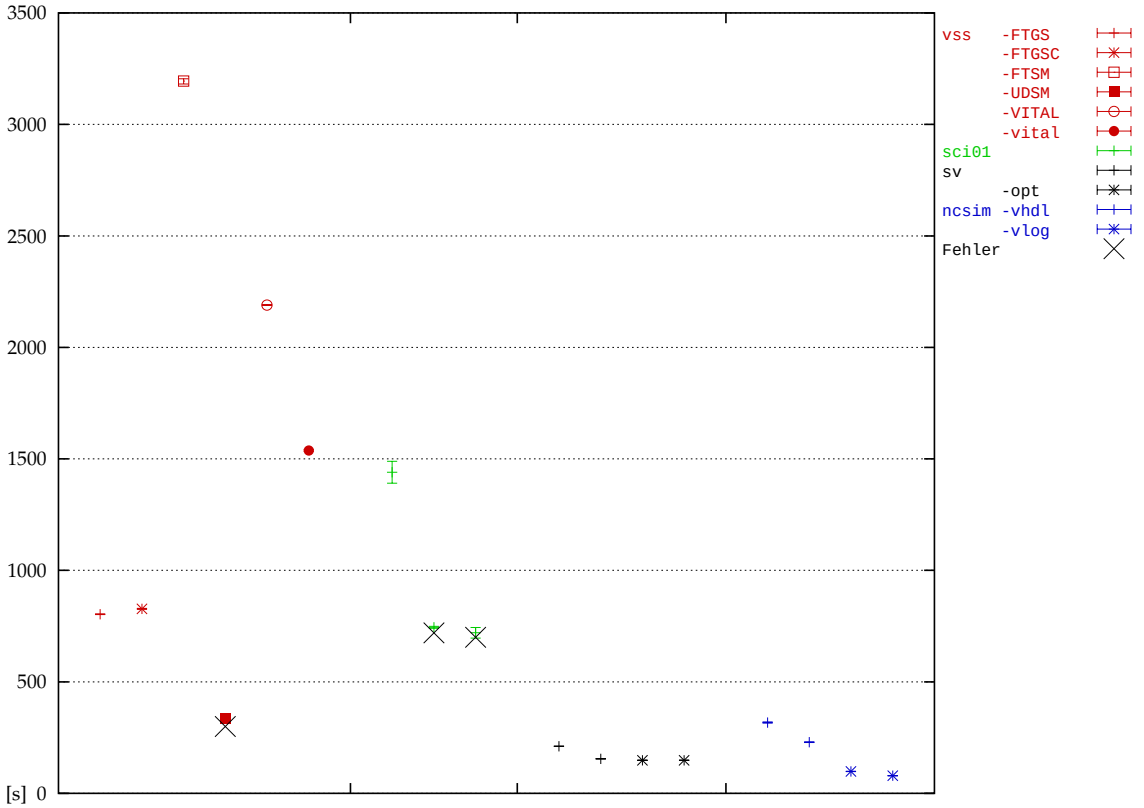
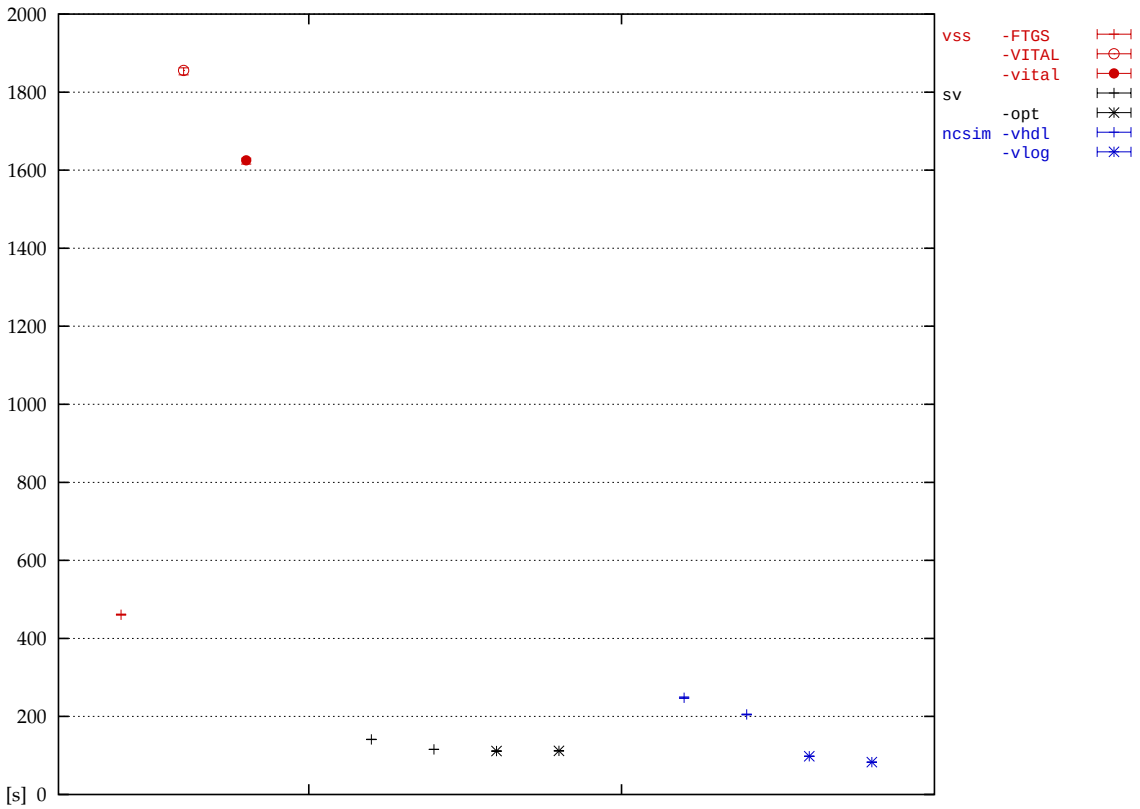


Tabelle 4: Operationswerk, UMC-Netzliste

Netzliste – VHDL						UMC-Prozess		
Simulator	avg. [s]	min.	max.	speed-up		Parameter		Fehler
VSS	460,67	459,72	462,49	3,53	3,34	vss.6	FTGS	
	1855,67	1844,18	1862,31	0,88	0,83	vss.6	VITAL	
	1625,18	1615,74	1630,84	∗	0,95	vss.6	vital	
Scirocco '02	1277,01	1268,14	1285,88	0,19	1,2	scs.2	VITAL	
	358,35	343,86	372,83	0,67	4,29	scs.3	VITAL	opw.1
	300,87	291,8	309,93	0,8	5,11	scs.4	VITAL	opw.1
	1206,79	1193,7	1219,87	0,2	1,27	scs.2	vital	
	359,64	355,37	363,91	0,67	4,27	scs.3	vital	opw.1
	240,75	239,94	241,56	∗	6,39	scs.4	vital	opw.1
Leapfrog	141,16	140,84	141,54	0,79	10,89	lea.2		
	115,67	115,6	115,72	0,97	13,29	lea.3		
	111,22	111,1	111,29	1,01	13,82	lea.2	opt	
	112,0	111,79	112,2	∗	13,73	lea.3	opt	
NCSim	248,04	246,3	249,93	0,33	6,2	ncs.2	vhdl	
	205,06	204,03	206,09	0,4	7,5	ncs.3	vhdl	
	97,92	97,62	98,47	0,85	15,7	ncs.2	vlog	
	82,84	82,68	82,93	∗	18,56	ncs.3	vlog	



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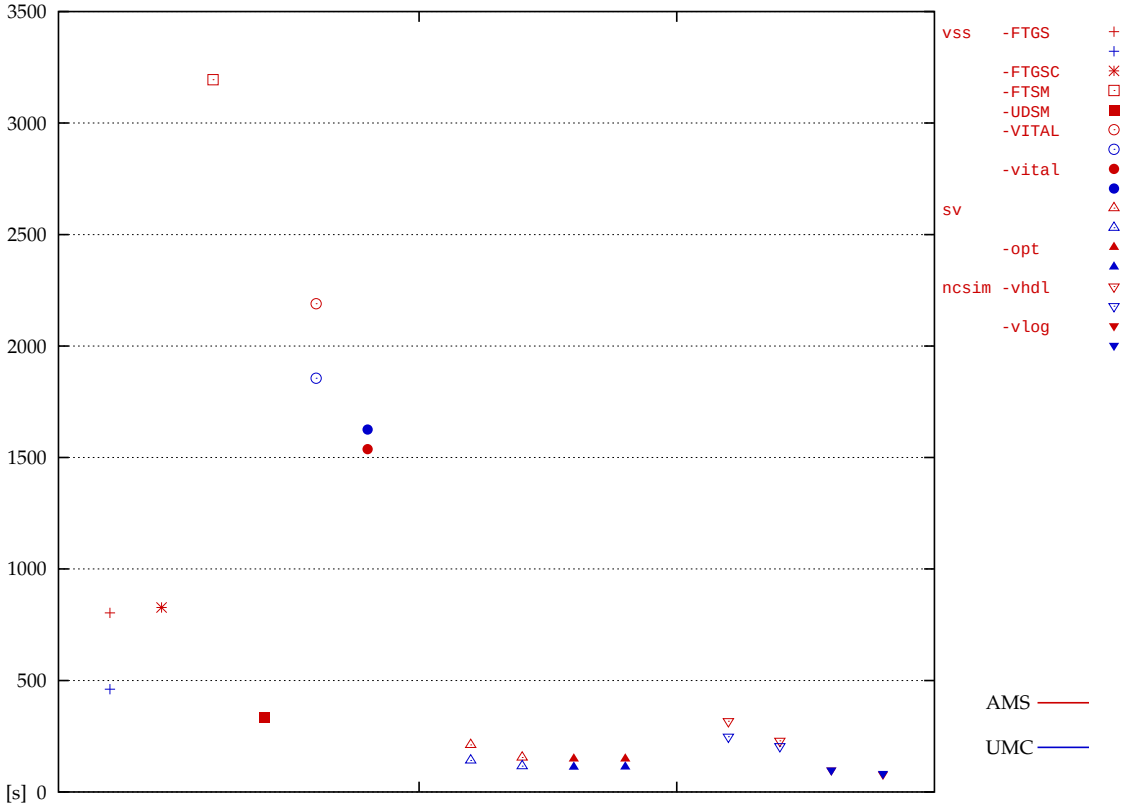


1.4 Netzliste, mixed-mode Simulation

Tabelle 5: Operationswerk, AMS-Netzliste, mixed-mode Simulation

Netzliste – VHDL + Verilog						AMS-Prozess	
Simulator	avg. [s]	min.	max.	speed-up		Parameter	Fehler
Scirocco	94,05	92,51	96,98	0,27	16,35	scm.1	
	84,62	82,4	88,99	0,3	18,17	scm.2	
	76,97	75,26	80,01	0,33	19,97	scm.3	
	38,64	37,48	40,95	0,65	39,79	scm.4	
	34,85	33,54	37,44	0,72	44,12	scm.5	
	25,2	24,37	26,82	∗	61,0	scm.6	
Scirocco '02	87,17	86,9	87,49	0,27	17,64	sms.1	
	79,21	78,2	81,03	0,3	19,41	sms.2	
	77,89	76,35	79,67	0,31	19,74	sms.3	
	48,88	48,68	49,12	0,49	31,45	sms.4	
	28,88	28,65	29,3	0,83	53,24	sms.5	
	23,89	23,62	24,38	∗	64,35	sms.6	
Leapfrog	537,38	536,79	538,07	0,8	2,86	lem.1	
	427,51	426,95	428,07	∗	3,6	lem.2	
NCSim	337,87	336,26	340,89	0,12	4,55	ncm.1	vhdl
	250,69	250,18	251,51	0,16	6,13	ncm.2	vhdl
	43,67	43,62	43,75	0,91	35,2	ncm.1	vlog
	39,6	39,53	39,65	∗	38,82	ncm.2	vlog

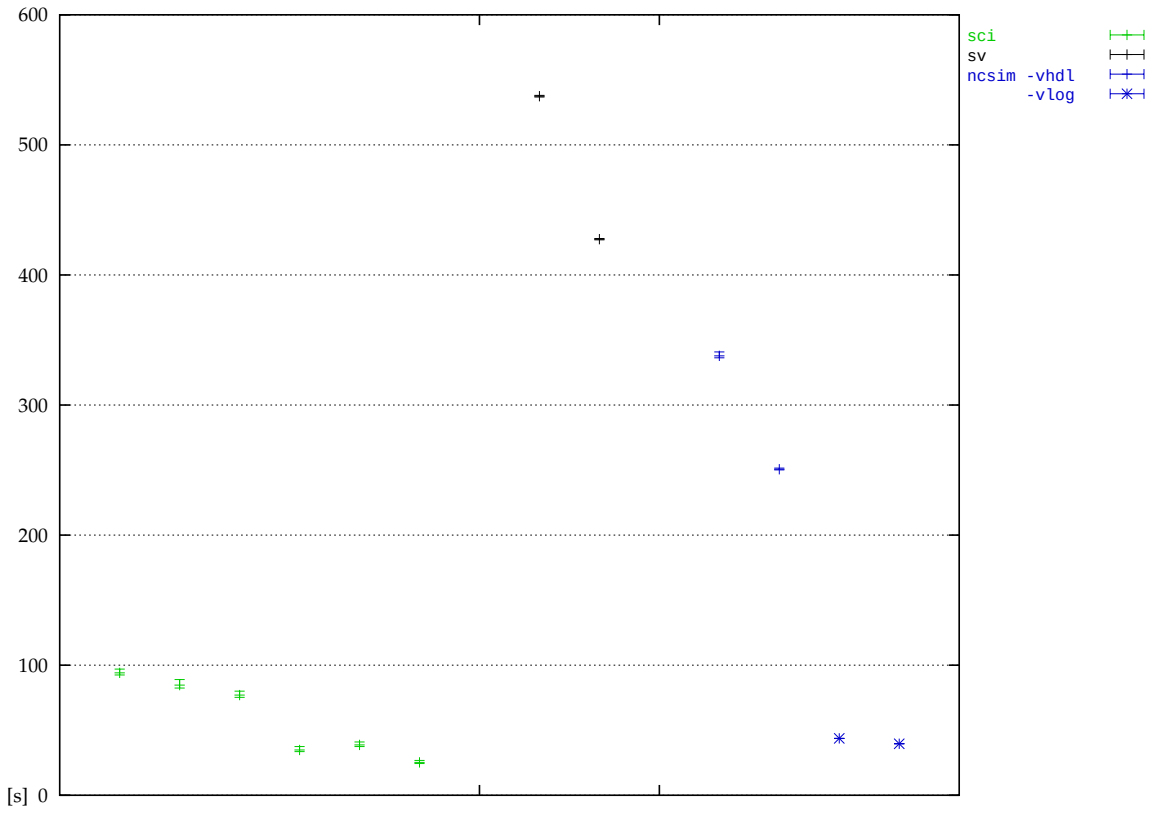
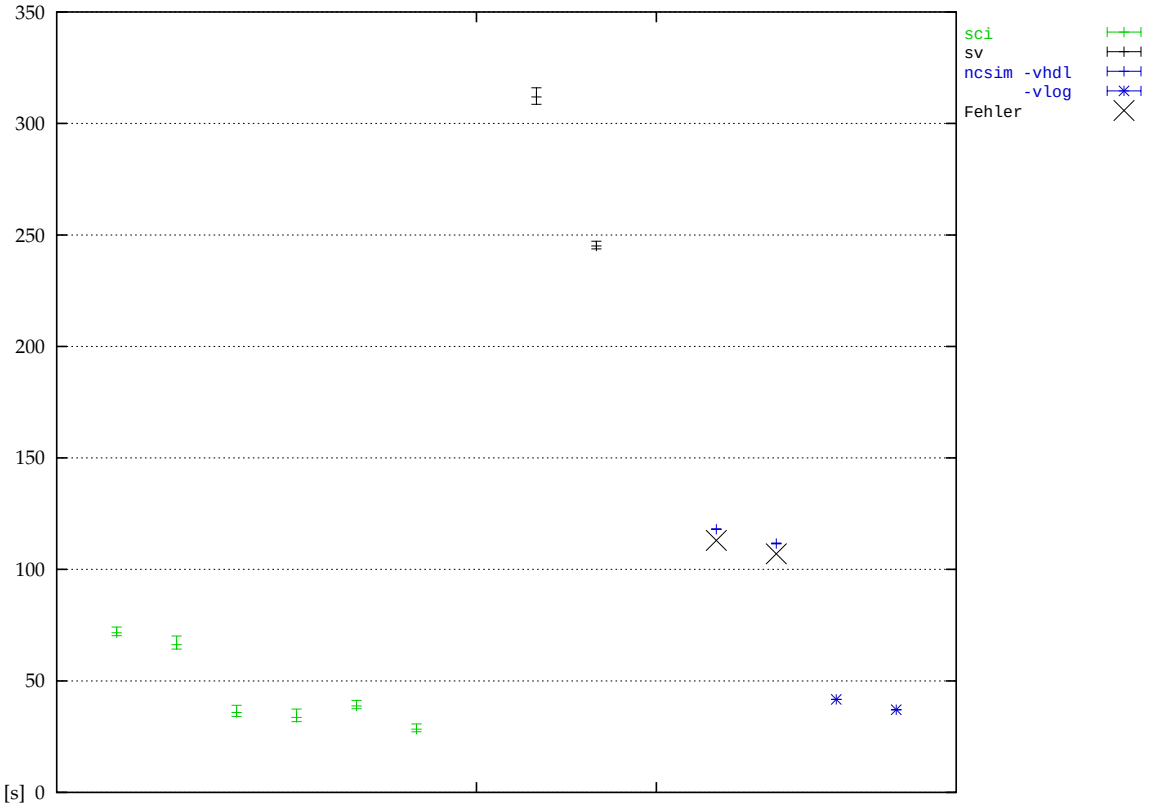


Tabelle 6: Operationswerk, UMC-Netzliste, mixed-mode Simulation

Netzliste – VHDL + Verilog						UMC-Prozess		
Simulator	avg. [s]	min.	max.	speed-up		Parameter		Fehler
Scirocco	71,6	70,26	74,18	0,4	21,47	scm.1		
	66,21	64,26	70,12	0,43	23,22	scm.2		
	35,81	34,09	39,09	0,79	42,93	scm.3		
	38,76	37,51	41,26	0,73	39,67	scm.4		
	33,63	31,75	37,35	0,84	45,72	scm.5		
	28,34	27,16	30,68	*	54,25	scm.6		
Scirocco '02	67,63	67,2	68,05	0,36	22,73	sms.1		
	57,91	57,44	58,64	0,42	26,55	sms.2		
	54,44	53,71	55,79	0,44	28,24	sms.3		
	35,61	35,5	35,68	0,68	43,17	sms.4		
	27,2	26,93	27,71	0,89	56,52	sms.5		
	24,2	24,13	24,25	*	63,53	sms.6		
Leapfrog	311,91	308,63	315,97	0,79	4,93	lem.1		
	245,04	243,73	247,15	*	6,27	lem.2		
NCSim	118,02	117,88	118,2	0,31	13,03	ncm.1	vhdl	opw.4
	111,63	111,44	111,83	0,33	13,77	ncm.2	vhdl	opw.4
	41,69	41,68	41,7	0,89	36,88	ncm.1	vlog	
	37,08	37,07	37,08	*	41,46	ncm.2	vlog	



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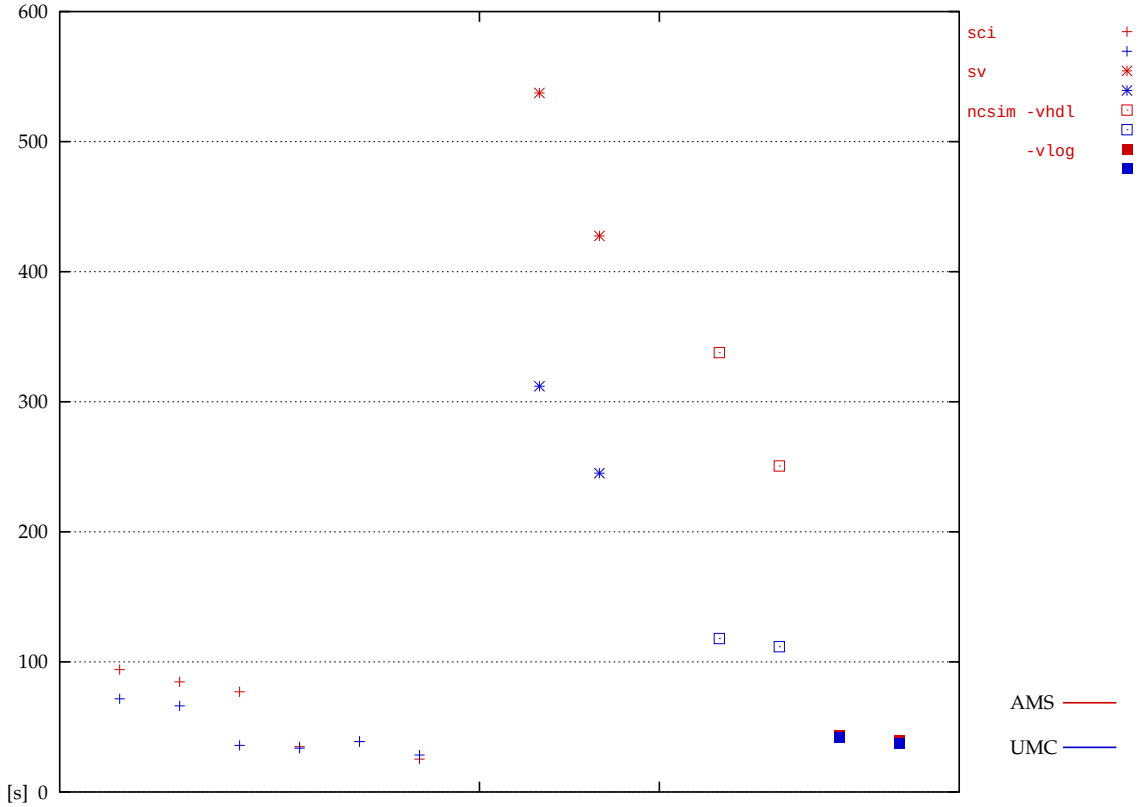


1.5 Netzliste, Verilog Simulation

Tabelle 7: Operationswerk, AMS-Netzliste, Verilog Simulation

Netzliste – Verilog						AMS-Prozess	
Simulator	avg. [s]	min.	max.	speed-up		Parameter	Fehler
VCS 6.2	64,51	64,05	65,32	0,47	23,83	vcs.4	
	58,35	58,24	58,44	0,52	26,35	vcs.5	
	57,6	53,12	63,07	0,53	26,69	vcs.6	
	32,76	30,31	37,29	0,93	46,93	vcs.7	
	21,1	21,0	21,16	1,45	72,86	vcs.8	
	30,53	30,42	30,73	∗	50,36	vcs.9	
Verilog	289,2	288,46	290,28	0,59	5,32	ver.1	
	170,9	170,18	171,57	∗	9,0	ver.2	
NCSim	40,54	40,38	40,68	0,88	37,92	ncv.2	
	35,87	35,83	35,9	∗	42,86	ncv.3	

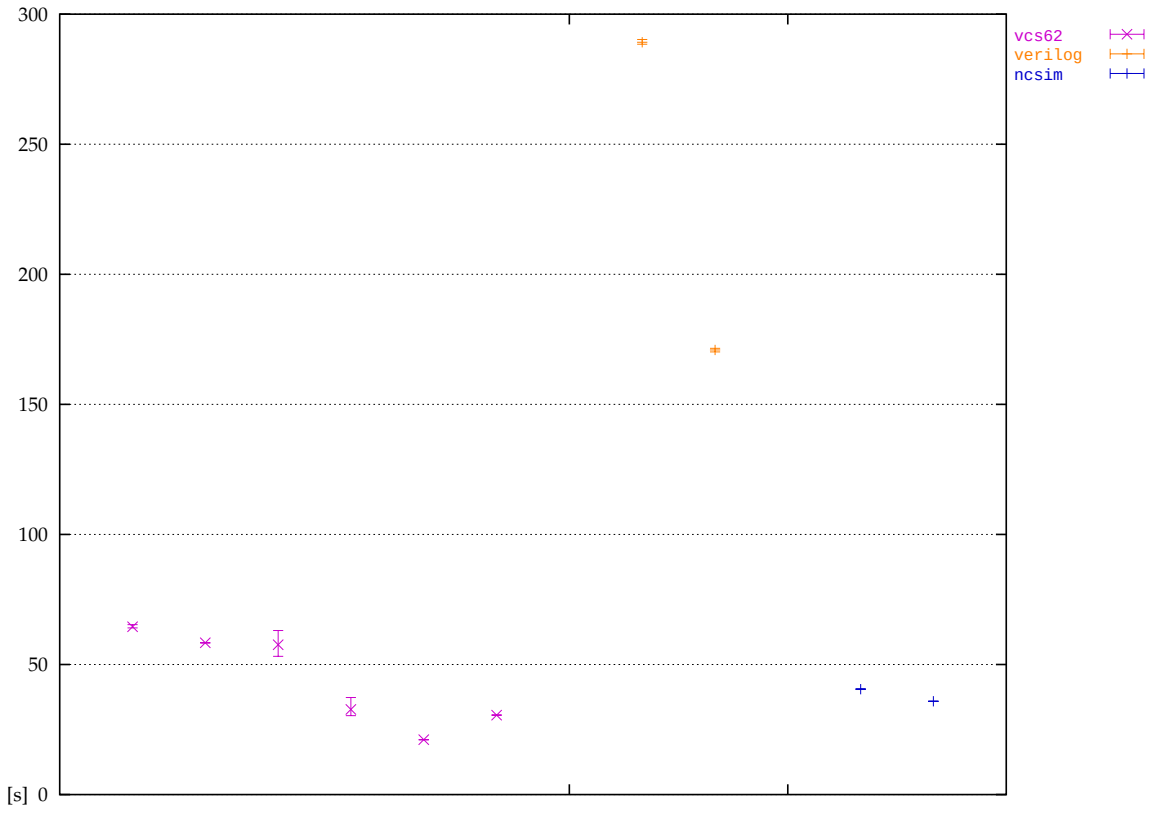
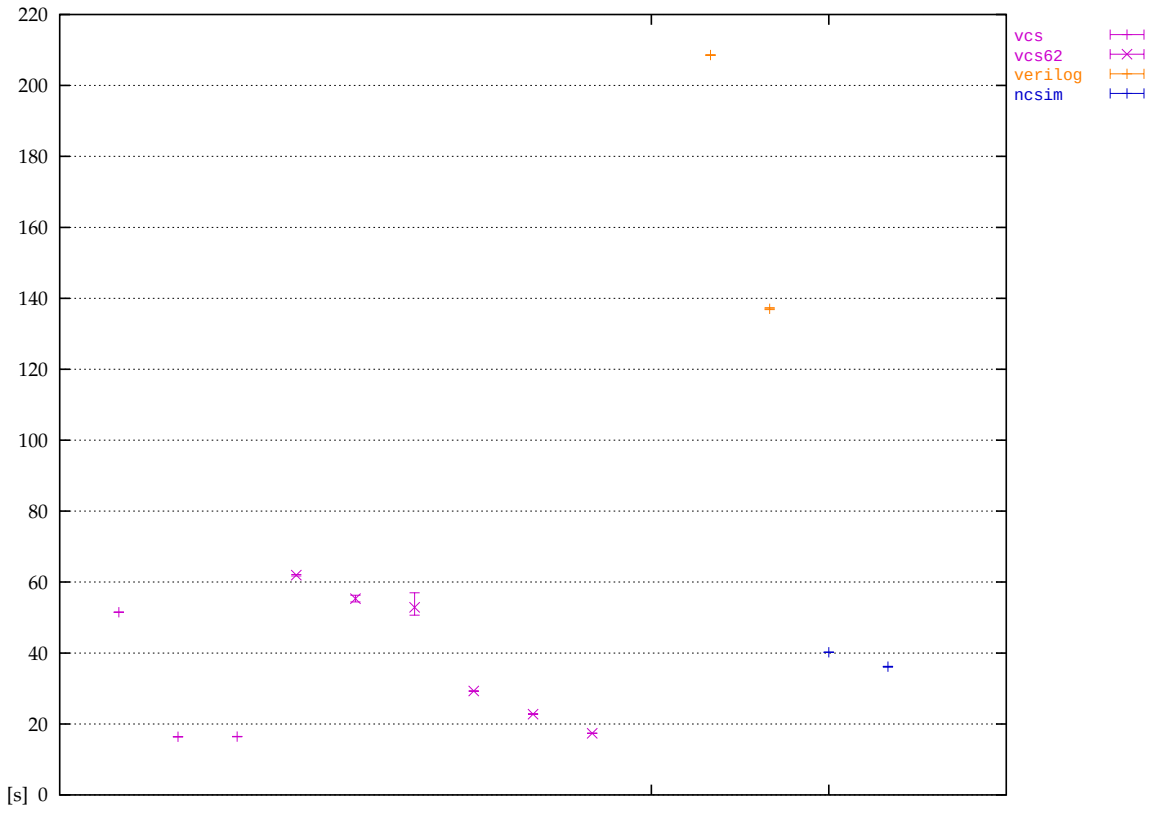
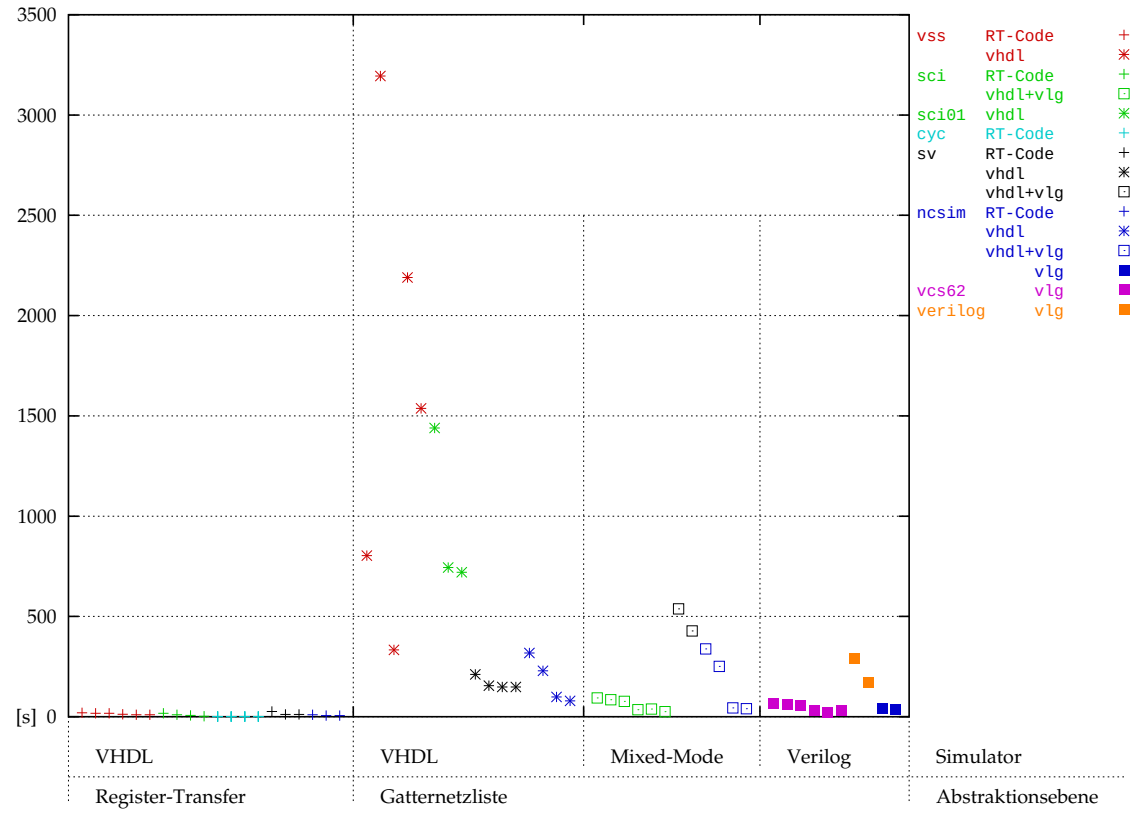


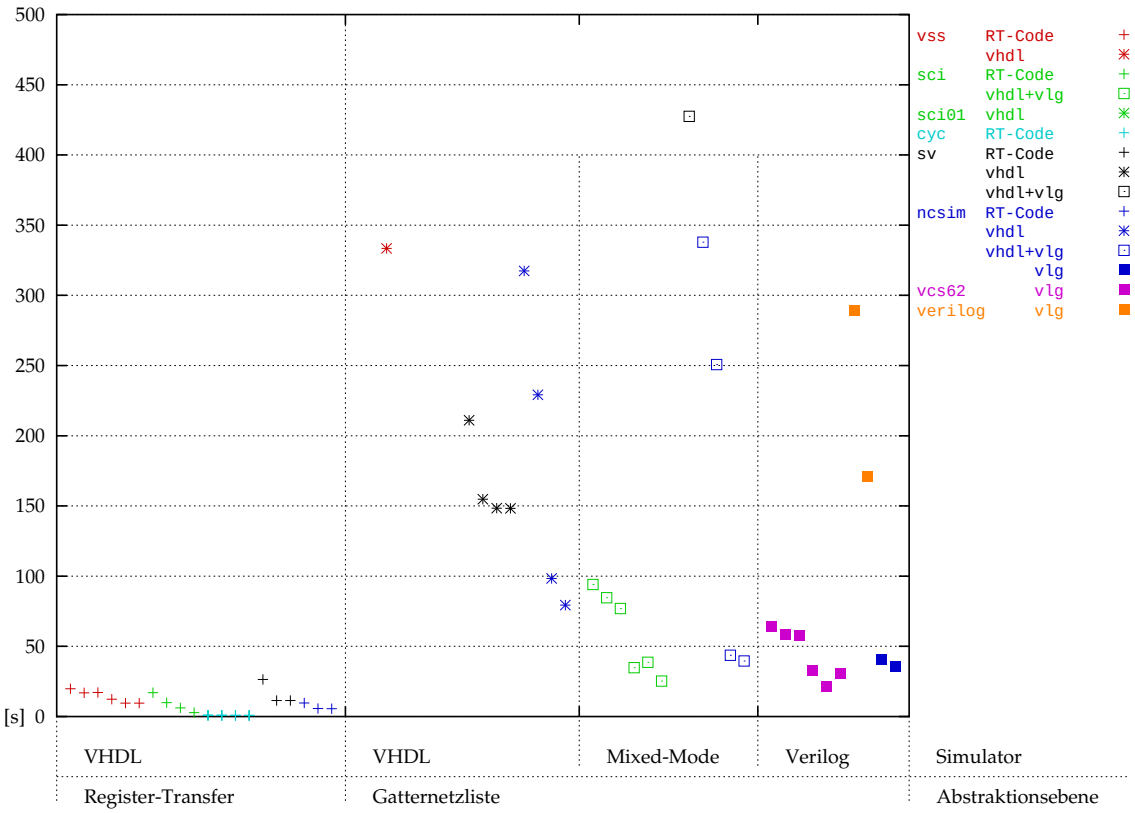
Tabelle 8: Operationswerk, UMC-Netzliste, Verilog Simulation

Netzliste – Verilog						UMC-Prozess	
Simulator	avg. [s]	min.	max.	speed-up		Parameter	Fehler
VCS	51,5	51,46	51,56	0,32	29,85	vcs.1	
	16,41	16,39	16,42	1,0	93,69	vcs.2	
	16,46	16,41	16,51	∗	93,4	vcs.3	
VCS 6.2	61,97	61,71	62,12	0,28	24,81	vcs.4	
	55,31	54,38	56,3	0,31	27,8	vcs.5	
	52,87	50,65	56,97	0,33	29,08	vcs.6	
	29,28	29,25	29,31	0,59	52,51	vcs.7	
	22,77	22,69	22,88	0,76	67,52	vcs.8	
	17,37	17,31	17,47	∗	88,51	vcs.9	
Verilog	208,59	208,5	208,64	0,66	7,37	ver.1	
	137,03	136,82	137,34	∗	11,22	ver.2	
NCSim	40,21	40,2	40,22	0,9	38,24	ncv.2	
	36,16	36,04	36,25	∗	42,52	ncv.3	



1.6 Übersicht



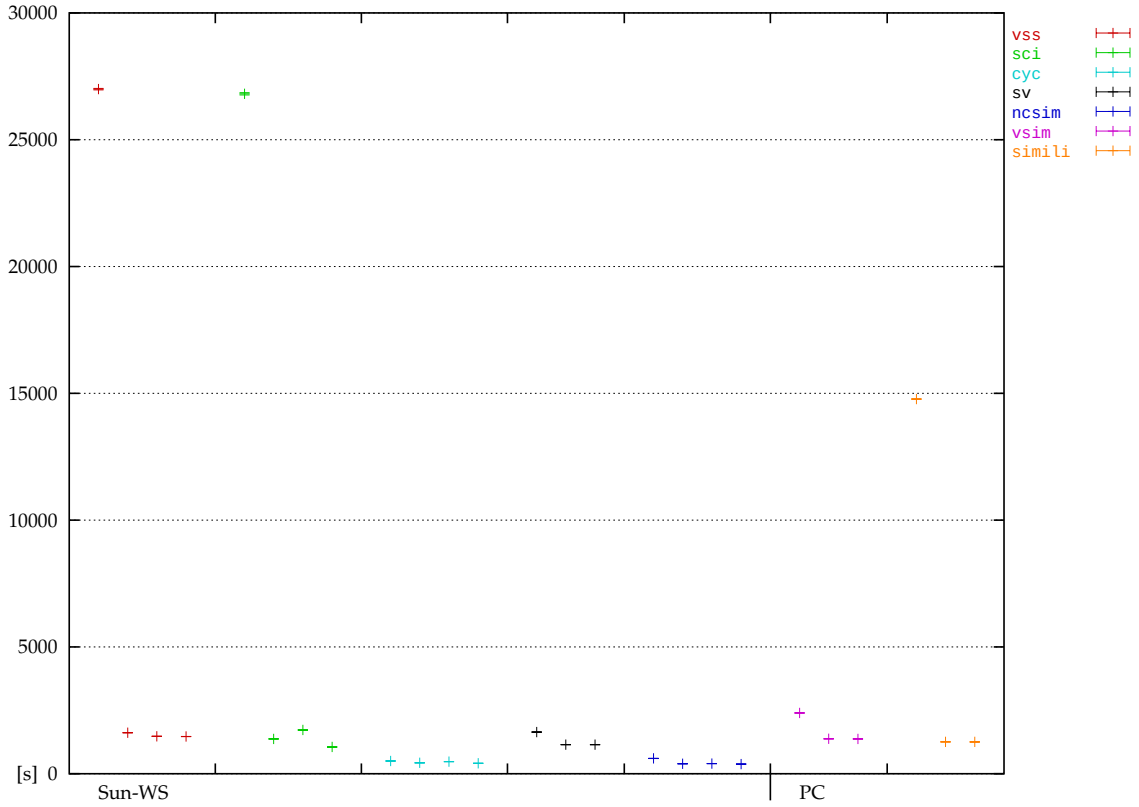


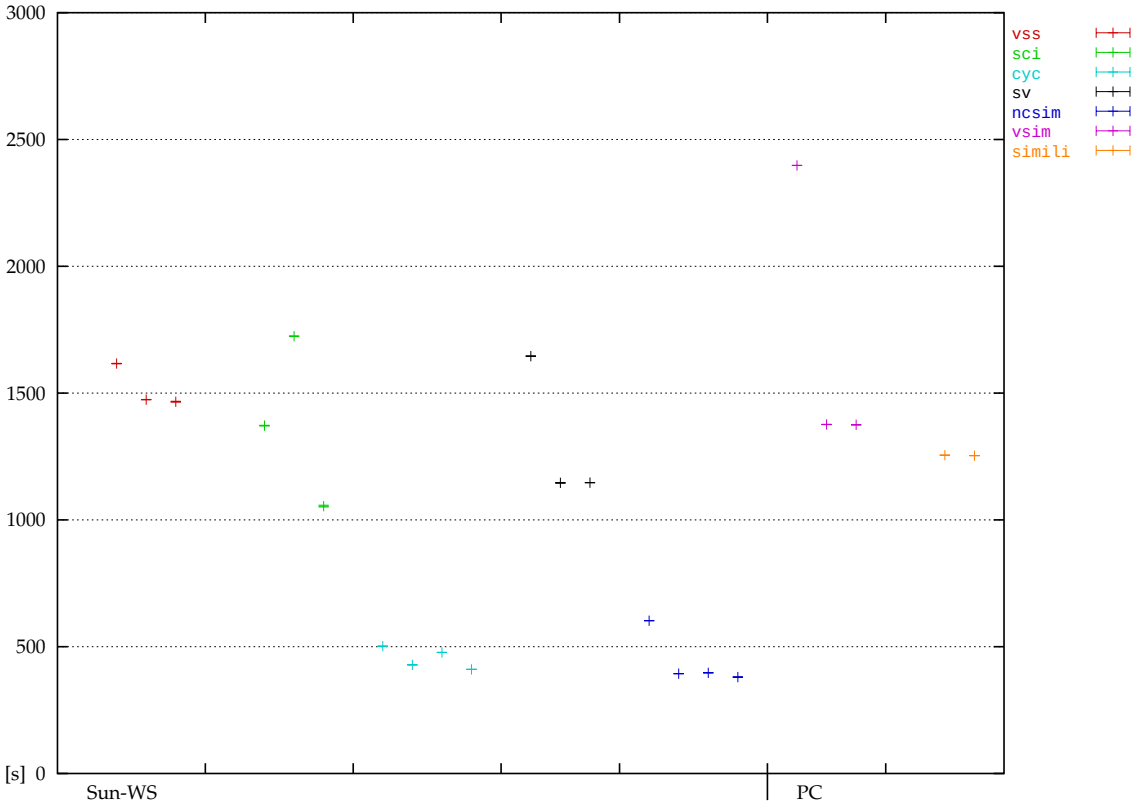
2 Funkwecker

2.1 Register-Transfer Beschreibung

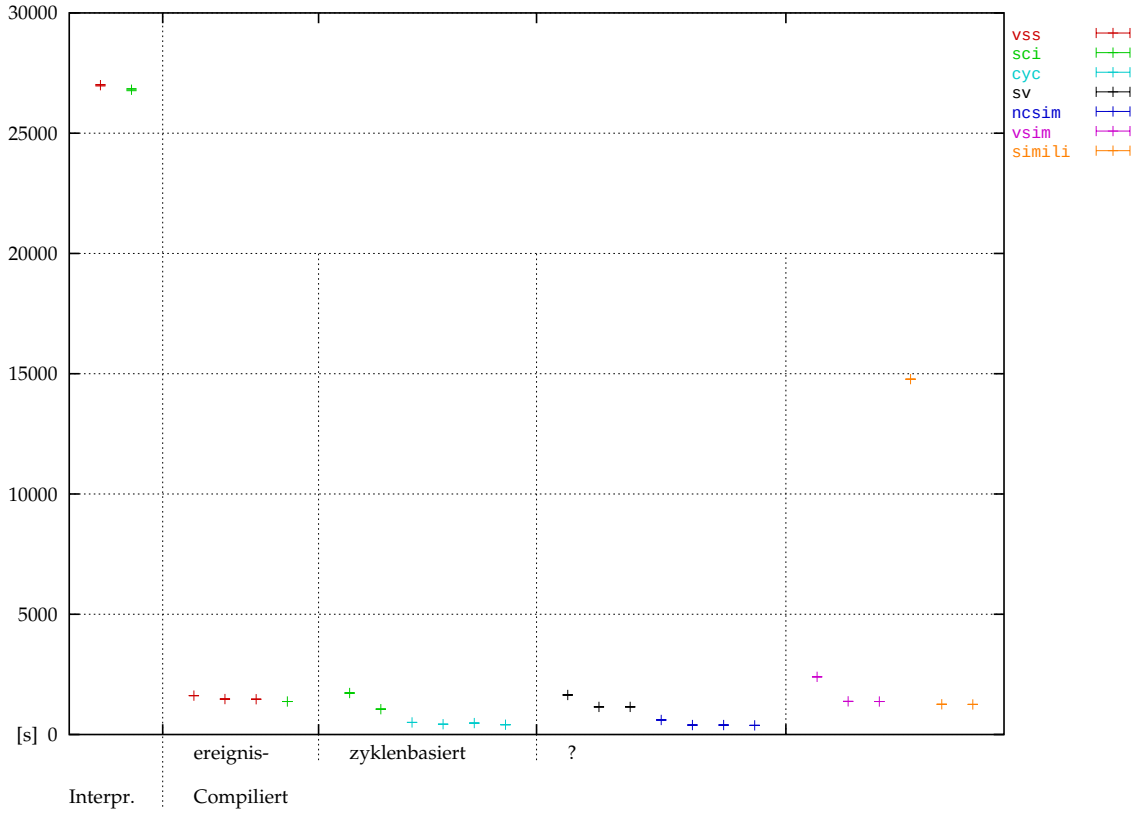
Tabelle 9: Funkwecker, RT-Code, Referenz zur Netzliste

Register-Transfer Code						Referenzzyklen	
Simulator	avg. [s]	min.	max.	speed-up		Parameter	Fehler
VSS	26995,04	26966,65	27023,42	0,05	1,32	vss.3	
	1616,33	1615,26	1617,39	0,91	22,12	vss.4	
	1474,22	1473,48	1474,96	0,99	24,25	vss.5	
	1466,02	1464,38	1467,66	$*$	24,38	vss.6	
Scirocco	26809,11	26763,59	26854,62	0,04	1,33	sci.1	
	1371,53	1370,22	1372,83	0,77	26,06	sci.2	
	1724,16	1722,81	1725,5	0,61	20,73	sci.3	
	1054,31	1050,82	1057,8	$*$	33,91	sci.4	
Cyclone	500,51	499,25	502,04	0,82	71,42	cyc.1	
	428,61	426,98	429,67	0,96	83,4	cyc.2	
	477,75	477,18	478,3	0,86	74,83	cyc.3	
	410,98	410,34	411,63	$*$	86,98	cyc.4	
Leapfrog	1645,6	1645,36	1645,83	0,7	21,72	lea.1	
	1146,0	1145,15	1146,85	1,0	31,19	lea.2	
	1146,83	1146,8	1146,86	$*$	31,17	lea.3	
NCSim	602,72	602,39	603,05	0,63	59,31	ncs.1	
	393,65	393,62	393,67	0,97	90,81	ncs.2	
	397,1	396,84	397,35	0,96	90,02	ncs.4	
	380,25	380,23	380,26	$*$	94,01	ncs.5	
ModelSim	2397,72	2397,39	2398,05	0,57		mod.1	
	1376,14	1375,55	1377,04	1,0		mod.2	
	1375,0	1374,51	1375,39	$*$		mod.3	
Simili	14772,93	14771,69	14774,18	0,08		sim.1	
	1254,92	1254,58	1255,3	1,0		sim.2	
	1253,31	1252,99	1253,87	$*$		sim.3	


30000
25000
20000
15000
10000
5000
[s] 0
Sun-WS
PC
vss
sci
cyc
sv
ncsim
vsim
simili


3000
2500
2000
1500
1000
500
[s] 0
Sun-WS
PC
vss
sci
cyc
sv
ncsim
vsim
simili

Funkwecker


30000
25000
20000
15000
10000
5000
[s] 0
vss
sci
cyc
sv
ncsim
vsim
simili
Interpr.
Compiliert
ereignis-
zyklenbasiert
?

2.2 Netzliste, VHDL Simulation

Tabelle 10: Funkwecker, AMS-Netzliste

Netzliste – VHDL						AMS-Prozess		
Simulator	avg. [s]	min.	max.	speed-up		Parameter		Fehler
VSS	22025,78	22025,66	22025,9	1,62	1,62	vss.6	FTGS	
	21573,1	21572,62	21573,57	1,62	1,62	vss.6	FTGSC	
	57005,68	57005,68	57005,68	0,63	0,63	vss.6	FTSM	clk.1
	4976,51	4973,03	4979,98	7,18	7,18	vss.6	UDSM	
	46290,66	46244,22	46337,09	0,77	0,77	vss.6	VITAL	
	35747,72	35745,72	35749,71	*	*	vss.6	vital	
Scirocco '01	28056,8	28048,54	28065,06	0,57	1,27	scs.2		
	17853,37	17828,68	17878,06	0,89	2,0	scs.3		clk.2
	15941,42	15876,19	16006,65	*	2,24	scs.4		clk.2
Leapfrog	34130,36	34128,07	34132,65	0,97	1,05	lea.2		
	32907,82	32902,02	32913,61	1,01	1,09	lea.3		
	33188,98	33186,46	33191,5	1,0	1,08	lea.2	opt	
	33179,83	33173,72	33185,93	*	1,08	lea.3	opt	
NCSim	5071,94	5065,12	5078,75	0,24	7,05	ncs.2	vhdl	
	2894,77	2894,63	2894,9	0,41	12,35	ncs.3	vhdl	
	1709,51	1709,39	1709,62	0,7	20,91	ncs.2	vlog	
	1193,28	1192,91	1193,64	*	29,96	ncs.3	vlog	

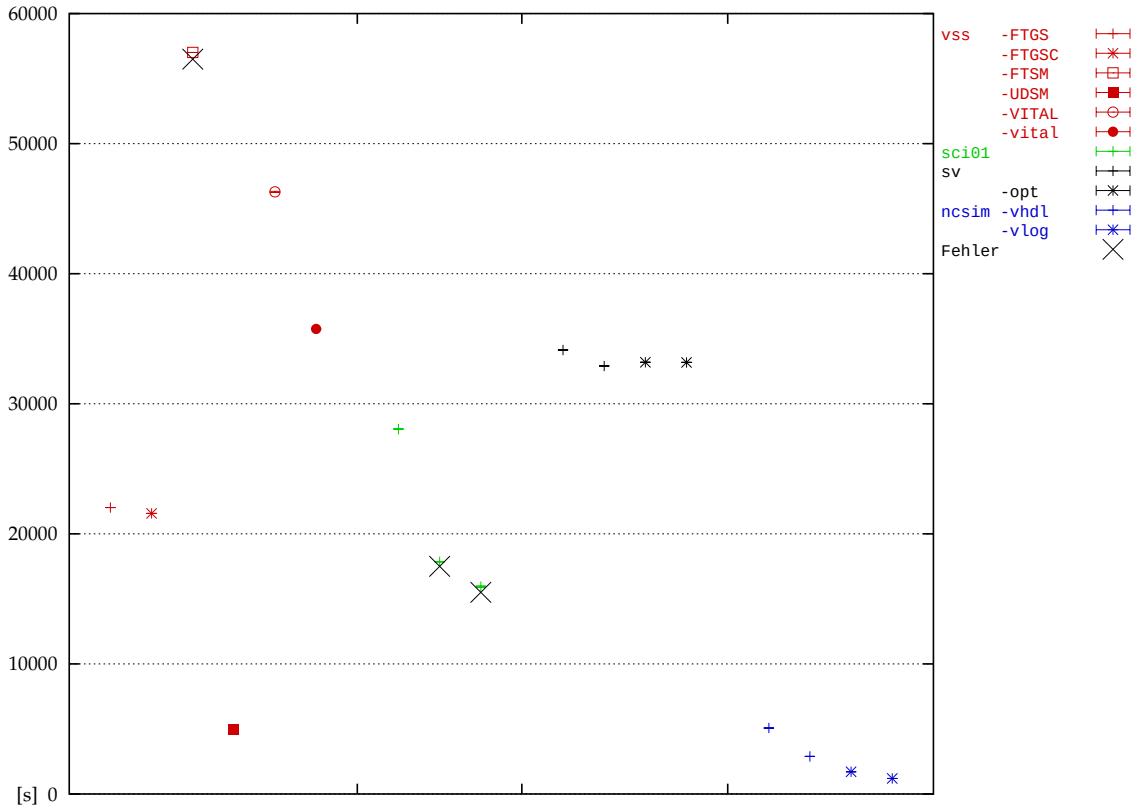
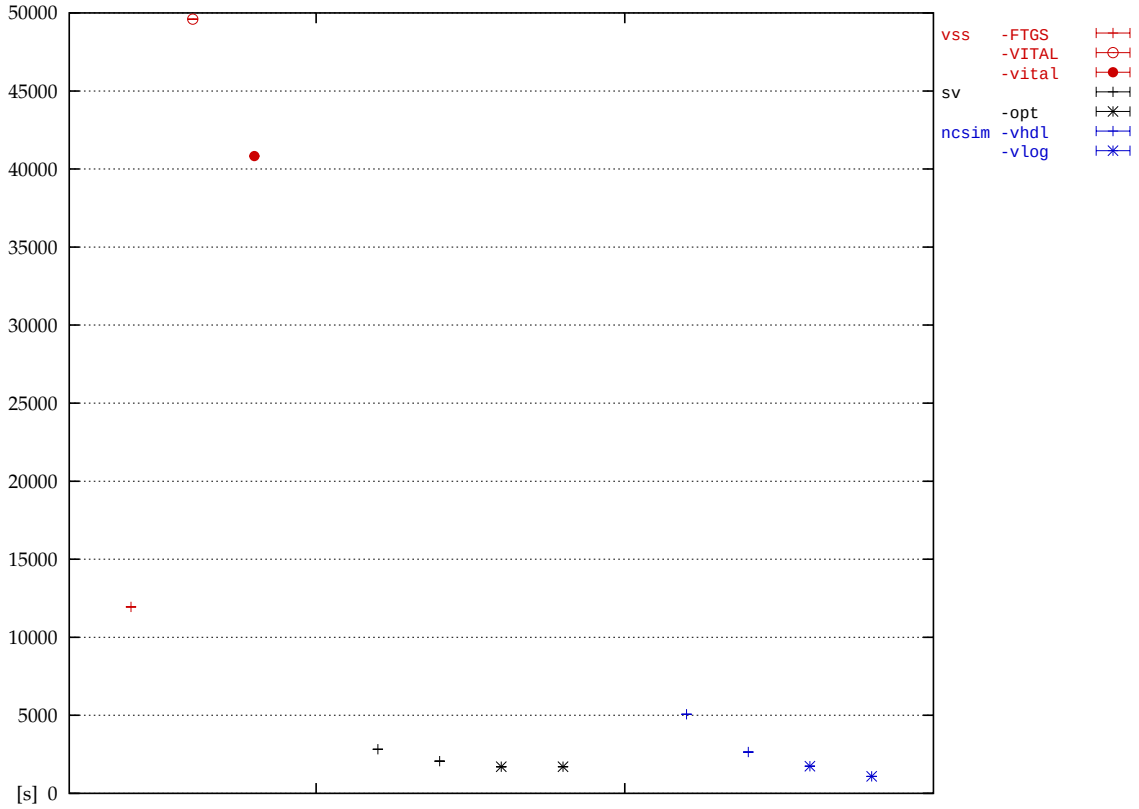
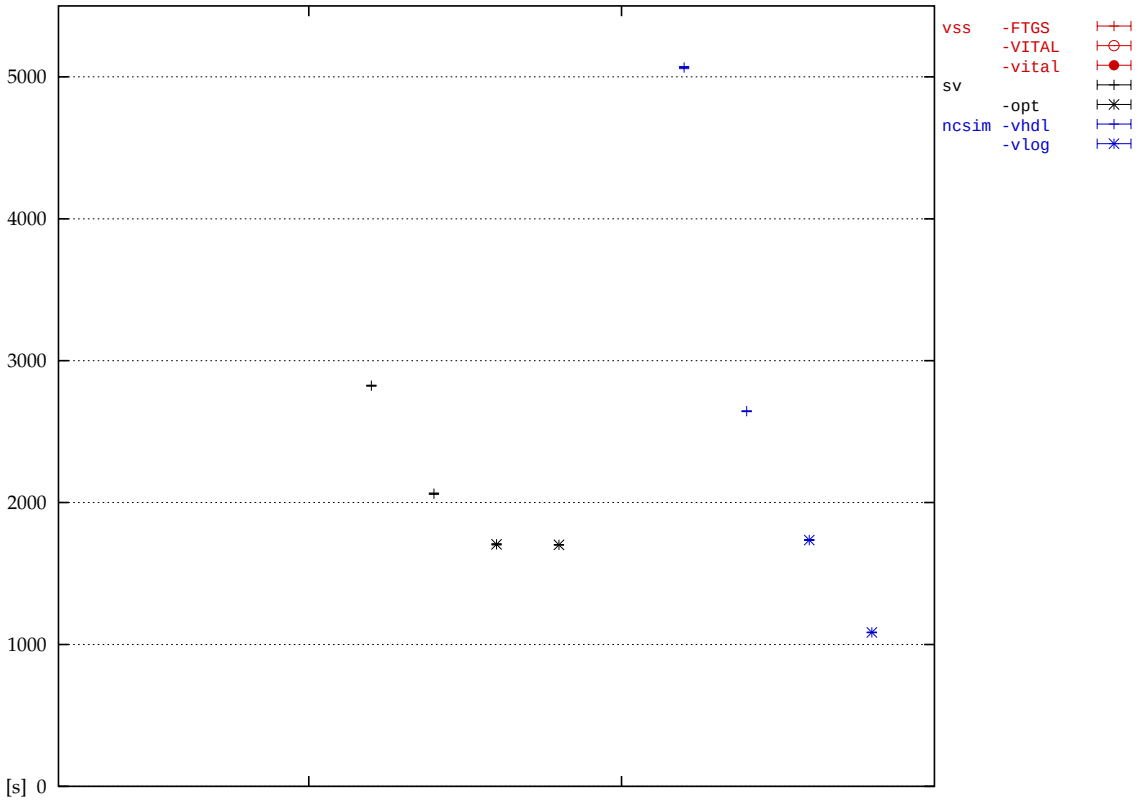


Tabelle 11: Funkwecker, UMC-Netzliste

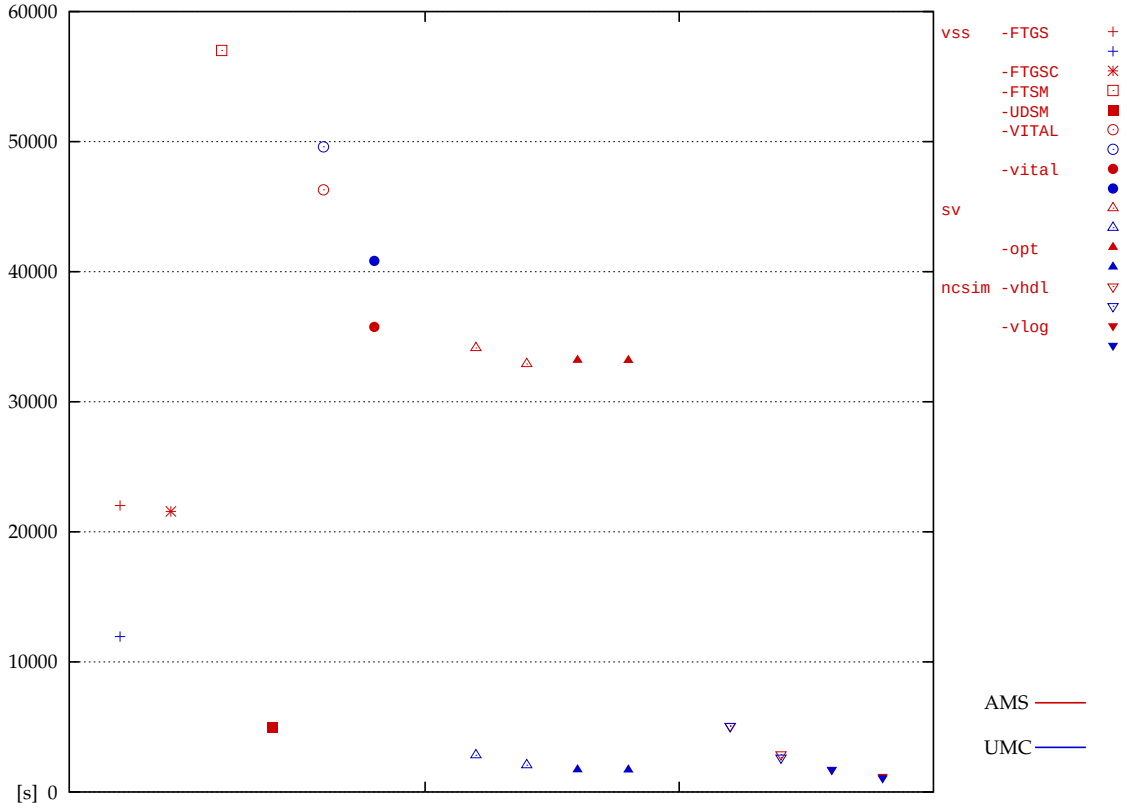
Netzliste – VHDL						UMC-Prozess	
Simulator	avg. [s]	min.	max.	speed-up		Parameter	Fehler
VSS	11944,22	11934,55	11953,88	3,42	2,99	vss.6	FTGS
	49602,35	49597,46	49607,24	0,82	0,72	vss.6	VITAL
	40829,06	40819,37	40838,75	∗	0,88	vss.6	vital
Leapfrog	2823,87	2820,08	2827,65	0,6	12,66	lea.2	
	2062,59	2058,27	2066,9	0,83	17,33	lea.3	
	1705,75	1700,85	1710,65	1,0	20,96	lea.2	opt
	1702,05	1701,46	1702,64	∗	21,0	lea.3	opt
NCSim	5065,32	5058,11	5072,52	0,21	7,06	ncs.2	vhdl
	2643,52	2640,47	2646,56	0,41	13,52	ncs.3	vhdl
	1735,77	1732,71	1738,82	0,63	20,59	ncs.2	vlog
	1085,19	1082,72	1087,65	∗	32,94	ncs.3	vlog



Funkwecker


5000
4000
3000
2000
1000
[s] 0
vss -FTGS
-VITAL
-vital
sv
-opt
ncsim -vhdl
-vlog

Vergleich der Gatterbibliotheken



2.3 Netzliste, mixed-mode Simulation

Tabelle 12: Funkwecker, AMS-Netzliste, mixed-mode Simulation

Netzliste – VHDL + Verilog						AMS-Prozess	
Simulator	avg. [s]	min.	max.	speed-up		Parameter	Fehler
Scirocco						scm	clk.3
Leapfrog	18867,97	18724,59	19011,34	0,82	1,89	lem.1	
	15401,76	15397,12	15406,39	*	2,32	lem.2	
NCSim	5587,15	5581,47	5592,83	0,11	6,4	ncm.1 vhdl	
	3221,93	3220,71	3223,15	0,19	11,1	ncm.2 vhdl	
	803,21	803,19	803,22	0,75	44,51	ncm.1 vlog	
	598,49	597,22	599,75	*	59,73	ncm.2 vlog	

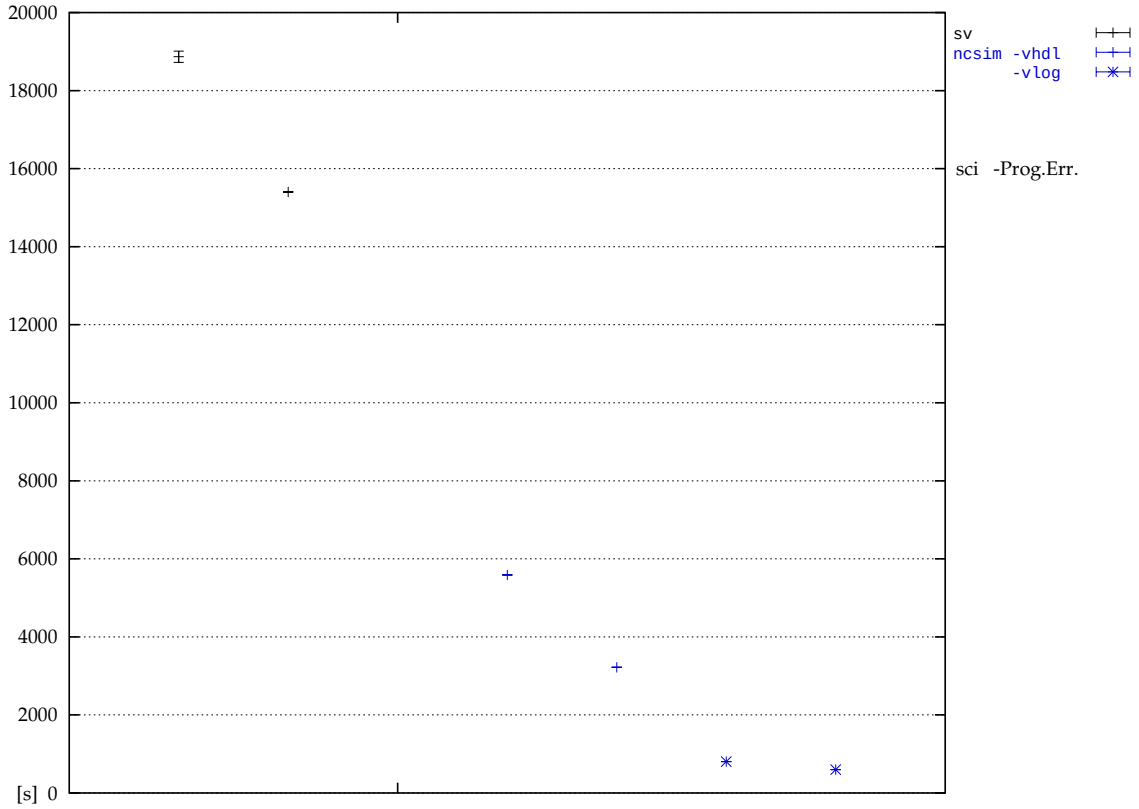
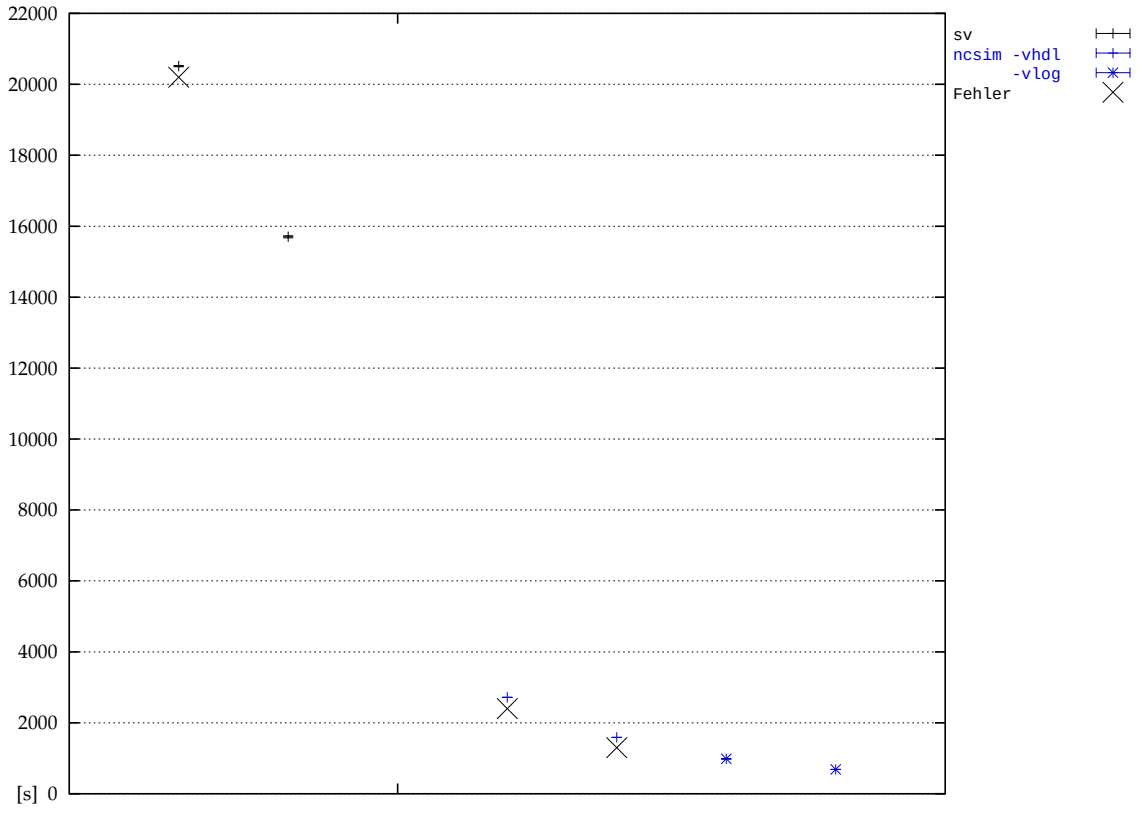
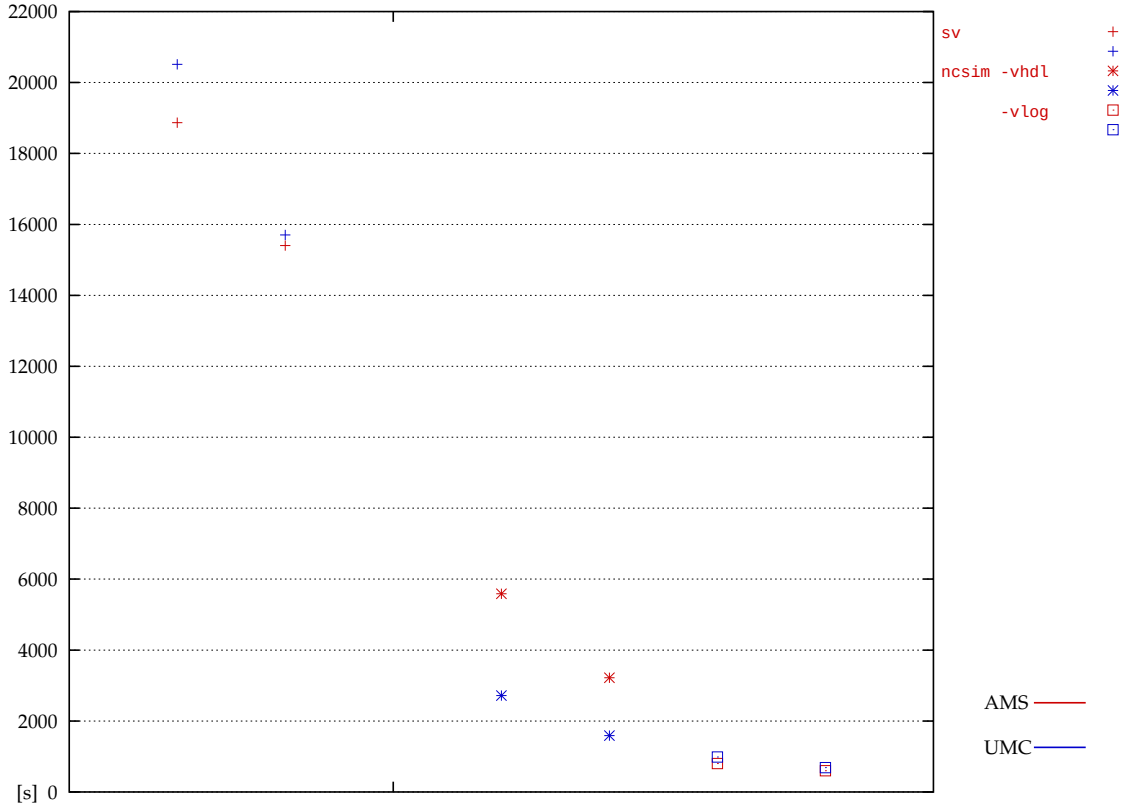


Tabelle 13: Funkwecker, UMC-Netzliste, mixed-mode Simulation

Netzliste – VHDL + Verilog						UMC-Prozess		
Simulator	avg. $[s]$	min.	max.	speed-up		Parameter		Fehler
Scirocco						scm		clk.3
Leapfrog	20511,76	20493,01	20530,5	0,77	1,74	lem.1		clk.4
	15701,47	15670,3	15732,63	$*$	2,28	lem.2		
NCSim	2718,65	2717,69	2719,6	0,25	13,15	ncm.1	vhdl	clk.5
	1588,21	1587,4	1589,02	0,43	22,51	ncm.2	vhdl	clk.5
	983,86	983,44	984,28	0,7	35,33	ncm.1	vlog	
	687,18	686,53	687,82	$*$	52,02	ncm.2	vlog	



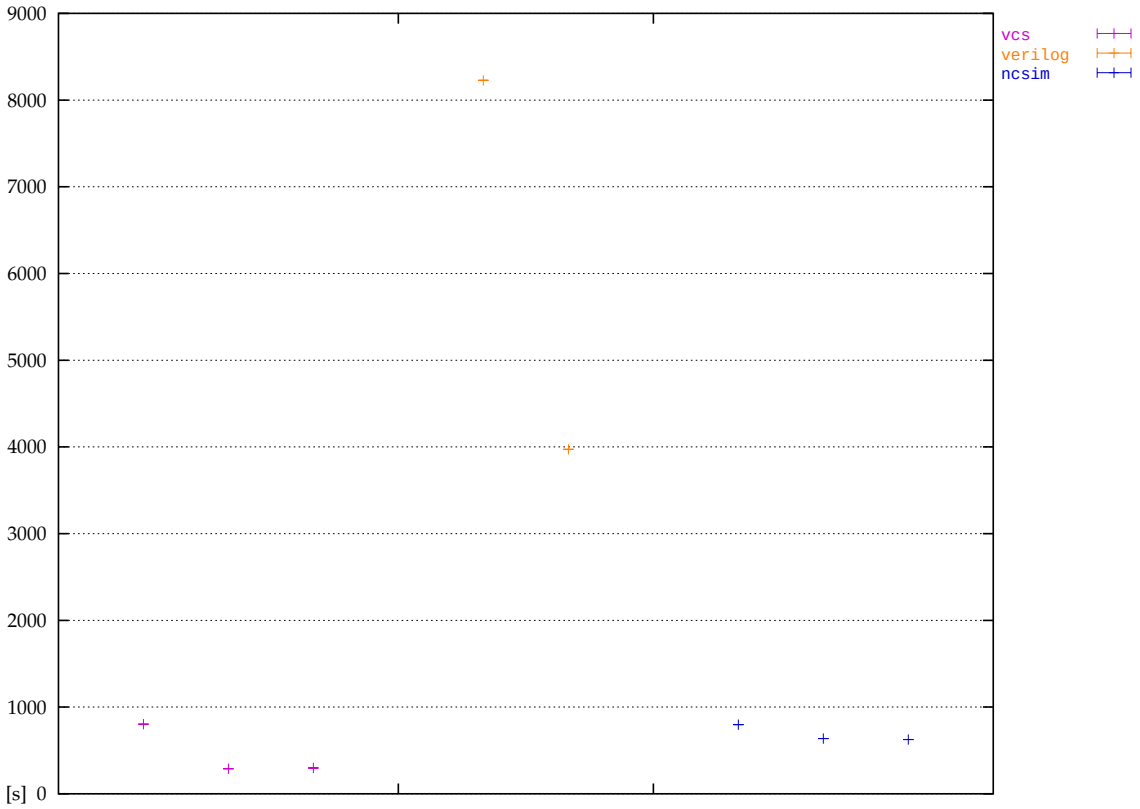
Vergleich der Gatterbibliotheken



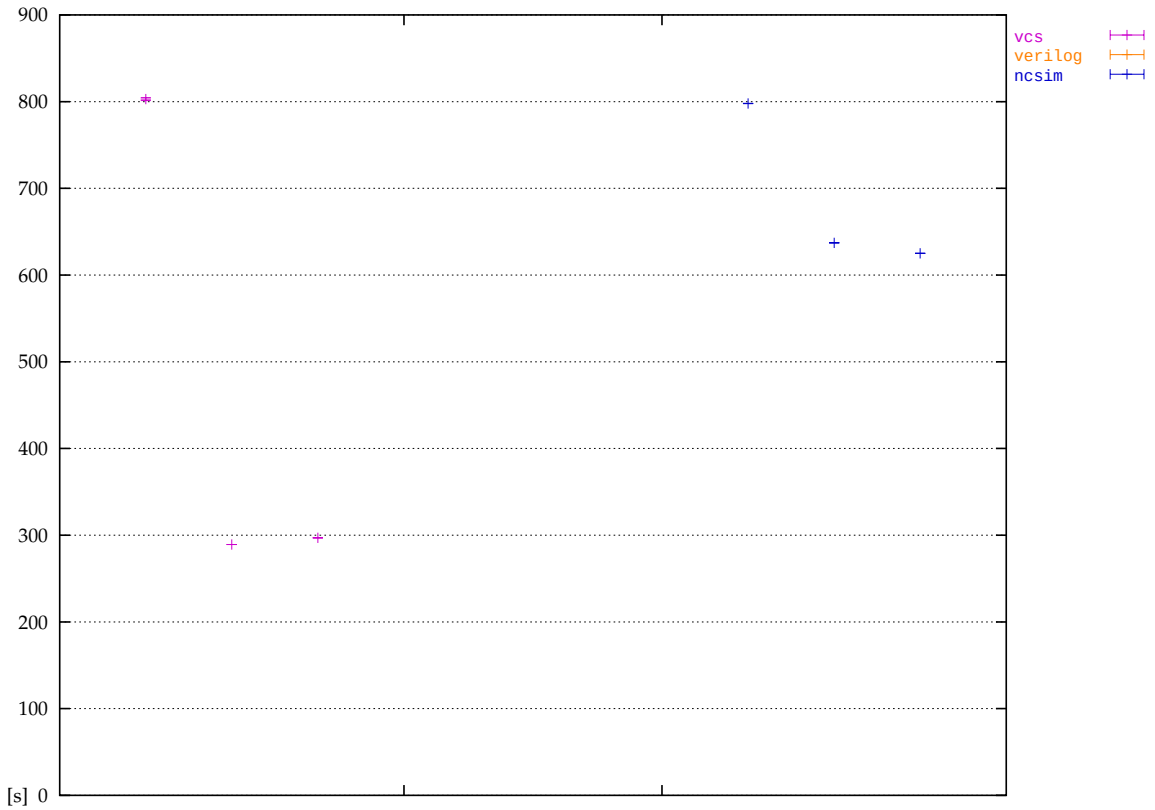
2.4 Netzliste, Verilog Simulation

Tabelle 14: Funkwecker, AMS-Netzliste, Verilog Simulation

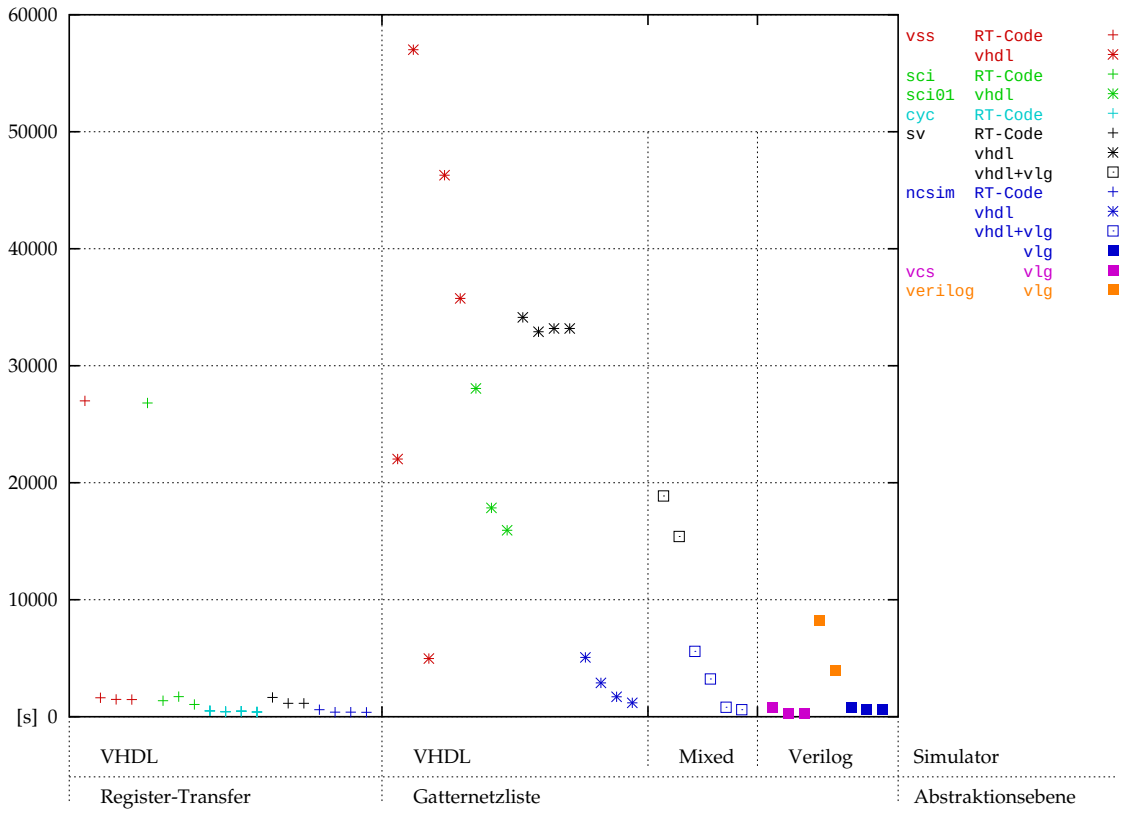
Netzliste – Verilog						AMS-Prozess	
Simulator	avg. [s]	min.	max.	speed-up		Parameter	Fehler
VCS	802,96	801,26	804,65	0,37	44,52	vcs.1	
	289,25	289,2	289,29	1,03	123,59	vcs.2	
	297,02	296,89	297,14	*	120,35	vcs.3	
Verilog	8228,11	8225,97	8230,25	0,48	4,34	ver.1	
	3972,34	3970,97	3973,7	*	9,0	ver.2	
NCSim	797,85	797,61	798,08	0,78	44,81	ncv.1	
	637,18	637,1	637,25	0,98	56,1	ncv.2	
	625,04	624,98	625,1	*	57,19	ncv.3	

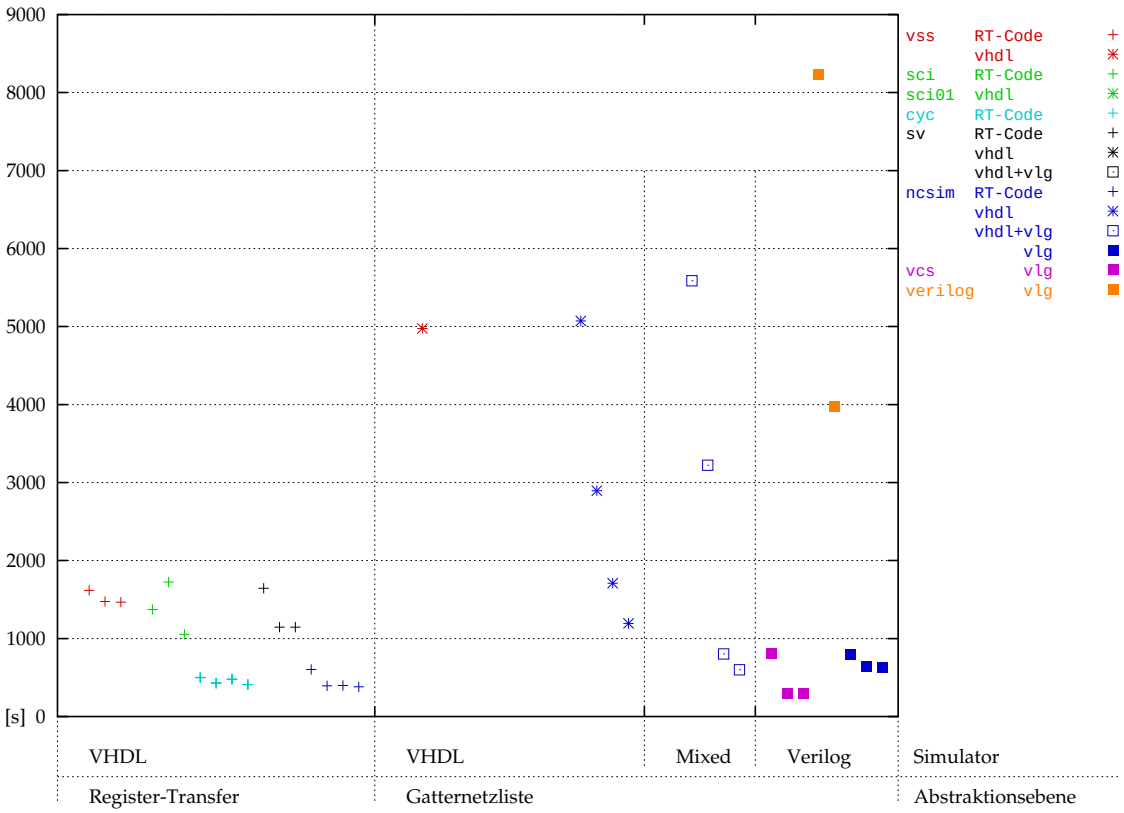


Funkwecker

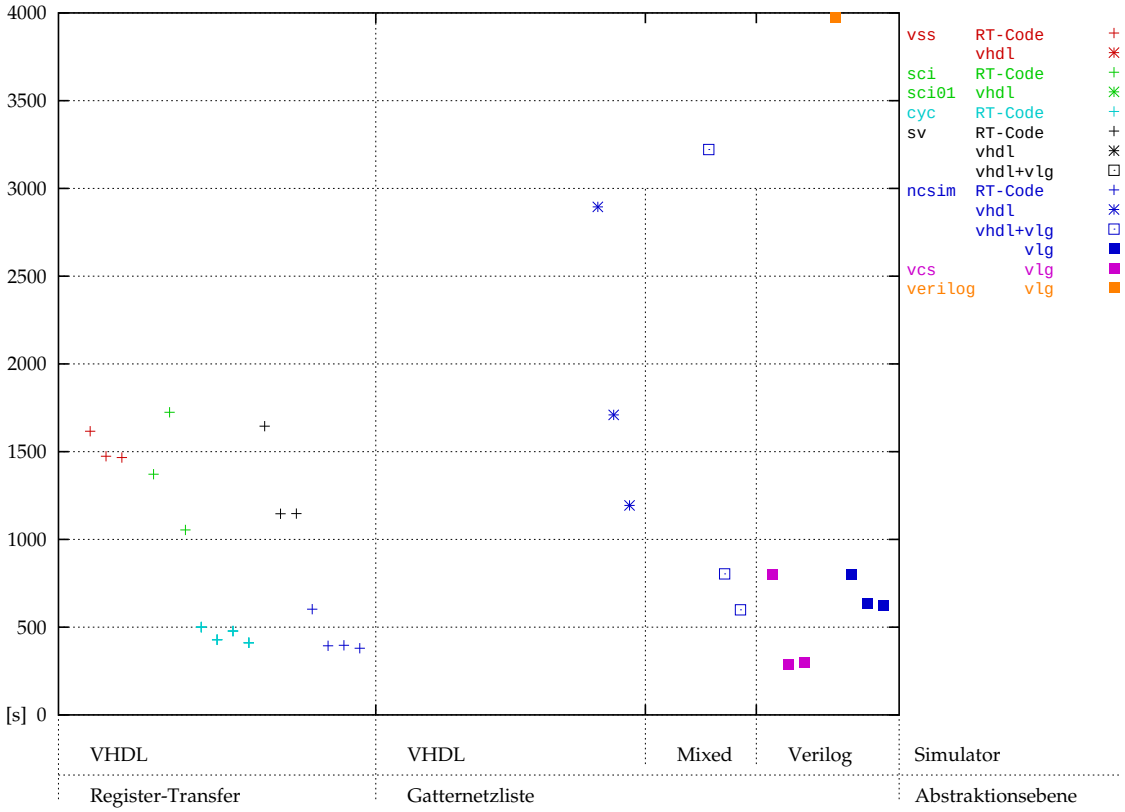


2.5 Übersicht





Funkwecker


4000
3500
3000
2500
2000
1500
1000
500
[s] 0
vss RT-Code
vhdl
sci RT-Code
sci01 vhdl
cyc RT-Code
sv RT-Code
vhdl
vhdl+vlg
ncsim RT-Code
vhdl
vhdl+vlg
vlg
vcs vlg
verilog vlg
VHDL
VHDL
Mixed
Verilog
Simulator
Register-Transfer
Gatternetzliste
Abstraktionsebene

3 Booth-Multiplizierer

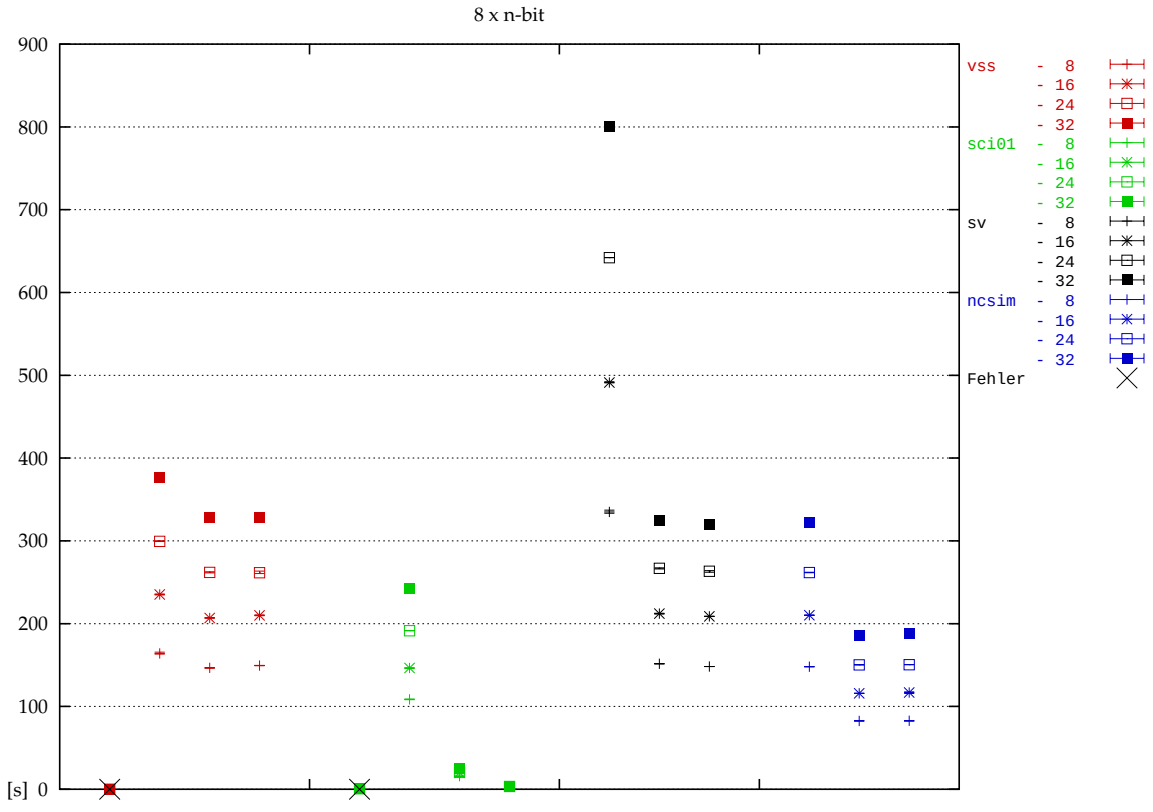
3.1 Register-Transfer Beschreibung

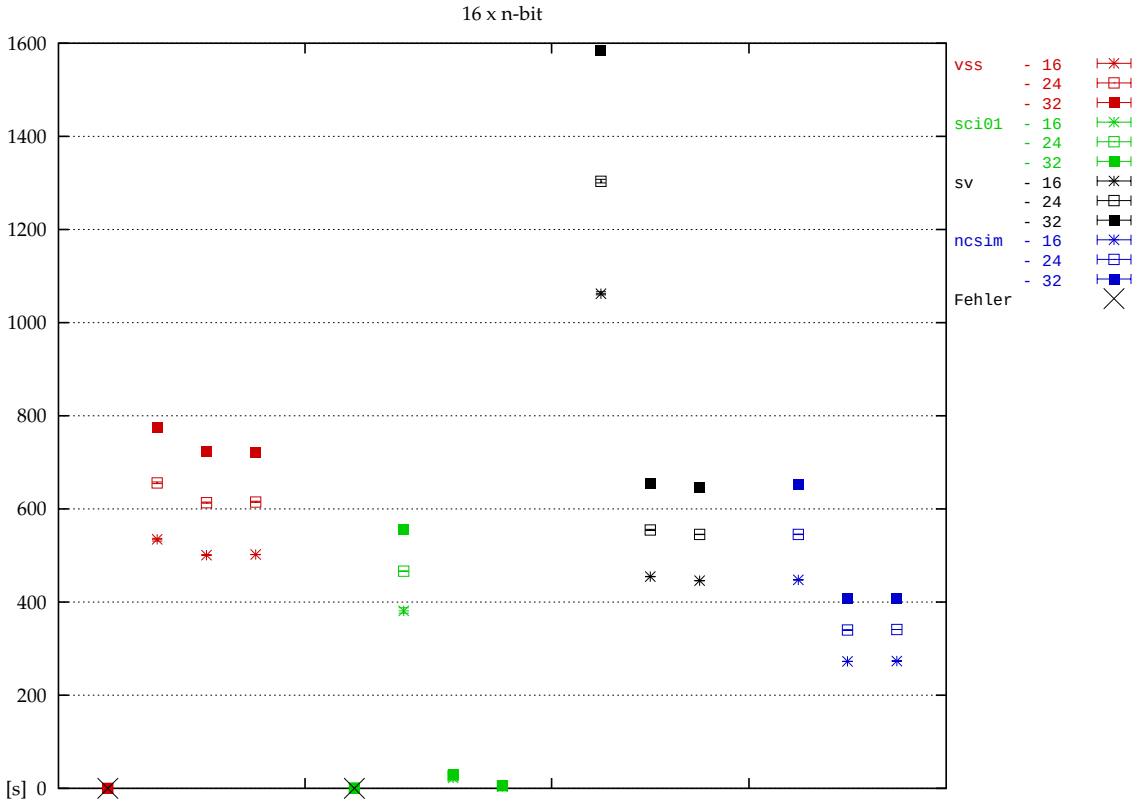
Tabelle 15: Booth-Multiplizierer, RT-Code

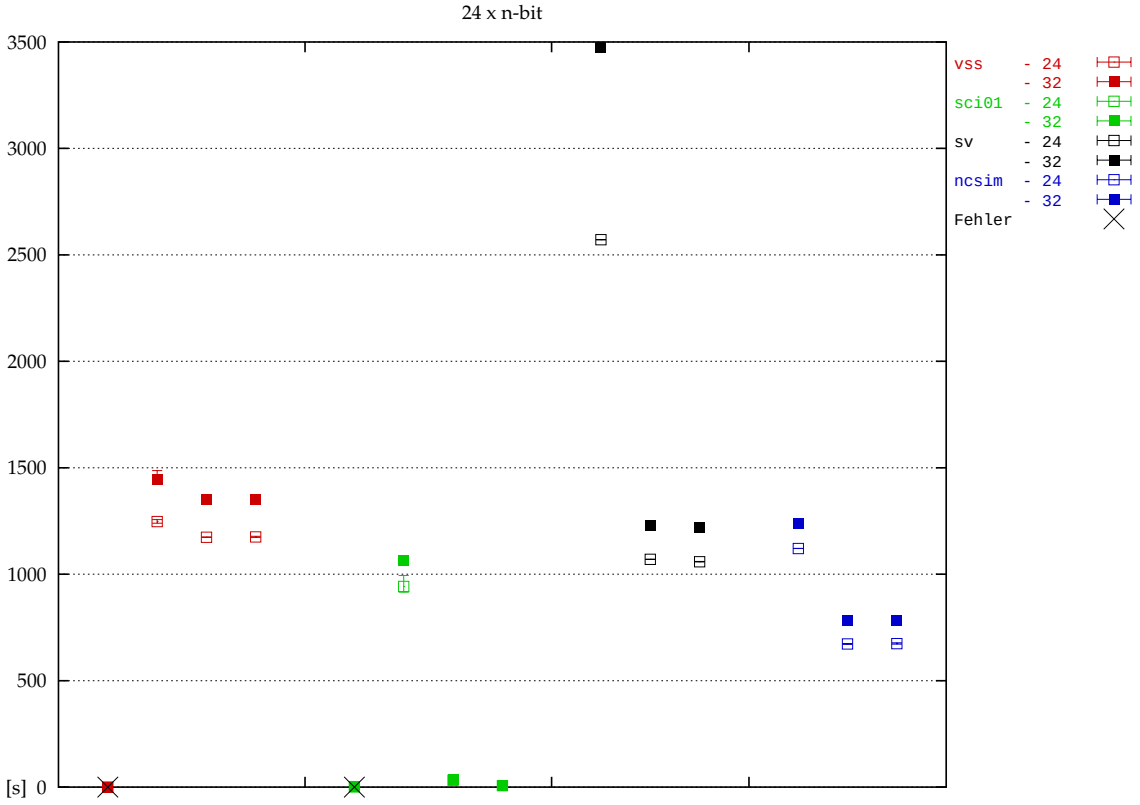
Register-Transfer Code						
Simulator	× 8 bit avg. [s]	× 16 bit avg. [s]	× 24 bit avg. [s]	× 32 bit avg. [s]	Parameter	Fehler
VSS					vss.3	mul.1
8 × ...	164,09	235,19	299,5	376,89	vss.4	
	146,65	206,9	261,86	328,16	vss.5	
	149,37	209,91	261,5	327,64	vss.6	
16 × ...		534,63	655,77	774,99	vss.4	
		500,87	613,23	723,19	vss.5	
		501,98	614,77	721,55	vss.6	
24 × ...			1246,9	1446,48	vss.4	
			1173,78	1349,05	vss.5	
			1174,8	1351,45	vss.6	
32 × ...				2252,73	vss.4	
				2147,55	vss.5	
				2141,96	vss.6	
Scirocco '01					scs.1	mul.1
8 × ...	108,49	146,36	191,5	242,84	scs.2	
	15,81	19,99	20,42	24,43	scs.3	
	3,33	3,27	3,33	3,79	scs.4	
16 × ...		381,12	466,25	555,41	scs.2	
		22,6	26,85	29,35	scs.3	
		3,75	5,67	5,87	scs.4	
24 × ...			942,58	1062,0	scs.2	
			32,59	35,75	scs.3	
			7,01	6,92	scs.4	
32 × ...				1703,44	scs.2	
				39,56	scs.3	
				9,31	scs.4	
Leapfrog	334,88	491,27	642,07	800,21	lea.1	
8 × ...	151,59	212,23	266,86	324,52	lea.2	
	148,26	208,83	263,29	320,35	lea.3	
16 × ...		1062,24	1303,61	1584,66	lea.1	
		454,85	554,58	655,18	lea.2	
		445,95	545,32	646,9	lea.3	
24 × ...			2570,93	3472,08	lea.1	
			1069,96	1227,69	lea.2	
			1058,71	1220,14	lea.3	
32 × ...				5479,53	lea.1	
				1931,08	lea.2	
				1908,47	lea.3	

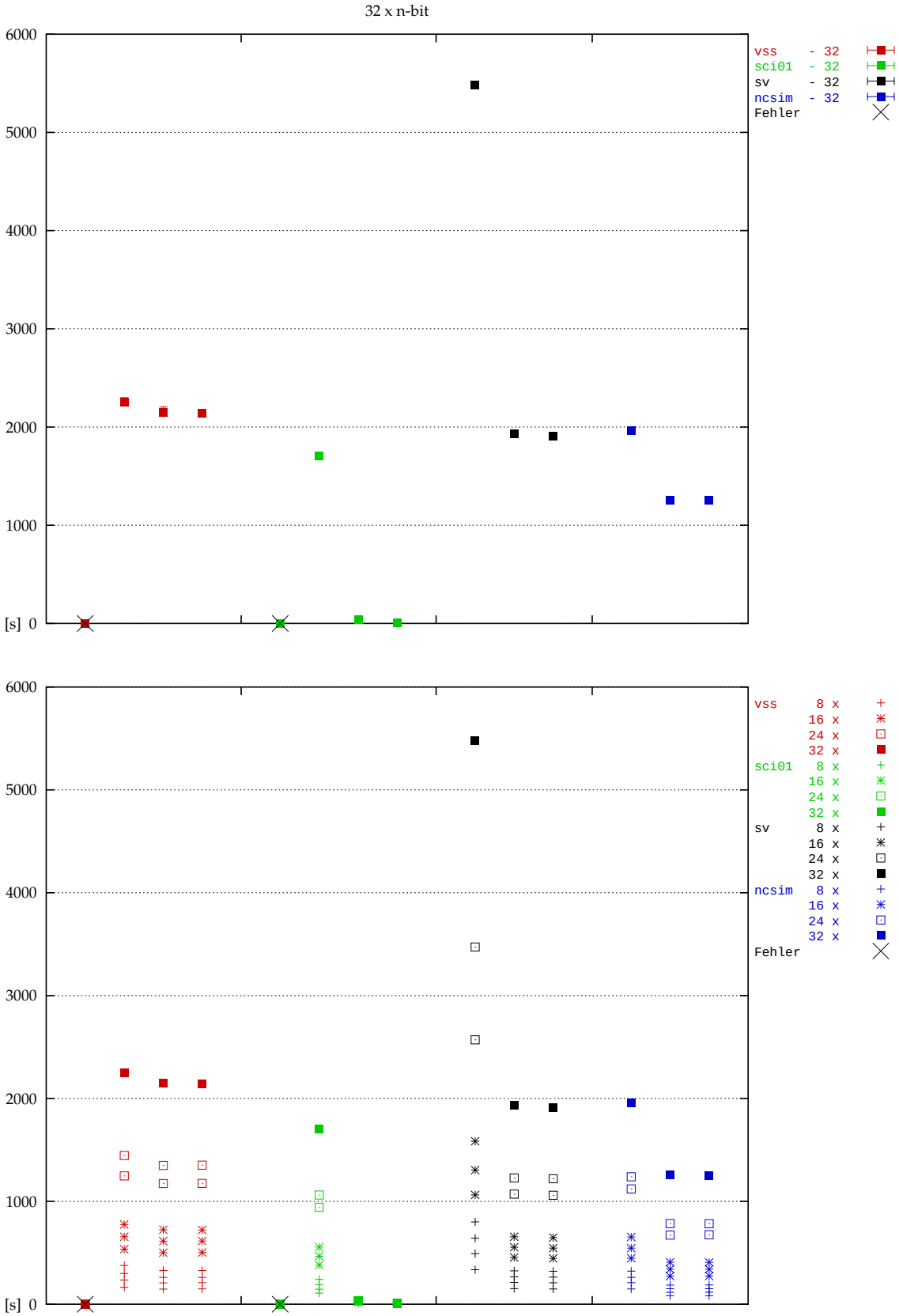
nächste Seite

Register-Transfer Code						
Simulator	× 8 bit avg. [s]	× 16 bit avg. [s]	× 24 bit avg. [s]	× 32 bit avg. [s]	Parameter	Fehler
NCSim	147,94	210,17	261,77	322,14	ncs.1	
8 × ...	82,58	115,81	150,25	185,54	ncs.2	
	82,68	116,93	150,49	187,79	ncs.3	
16 × ...		447,83	545,39	653,42	ncs.1	
		272,53	339,98	408,51	ncs.2	
		273,37	340,99	407,1	ncs.3	
24 × ...			1120,77	1238,63	ncs.1	
			672,47	784,33	ncs.2	
			674,11	782,28	ncs.3	
32 × ...				1960,96	ncs.1	
				1254,54	ncs.2	
				1253,92	ncs.3	




16 x n-bit
1600
1400
1200
1000
800
600
400
200
[s] 0
vss - 16
- 24
- 32
sci01 - 16
- 24
- 32
sv - 16
- 24
- 32
ncsim - 16
- 24
- 32
Fehler


24 x n-bit
3500
3000
2500
2000
1500
1000
500
[s] 0
vss - 24
- 32
sci01 - 24
- 32
sv - 24
- 32
ncsim - 24
- 32
Fehler


32 x n-bit
6000
5000
4000
3000
2000
1000
[s] 0
vss - 32
sci01 - 32
sv - 32
ncsim - 32
Fehler
vss 8 x
16 x
24 x
32 x
sci01 8 x
16 x
24 x
32 x
sv 8 x
16 x
24 x
32 x
ncsim 8 x
16 x
24 x
32 x
Fehler

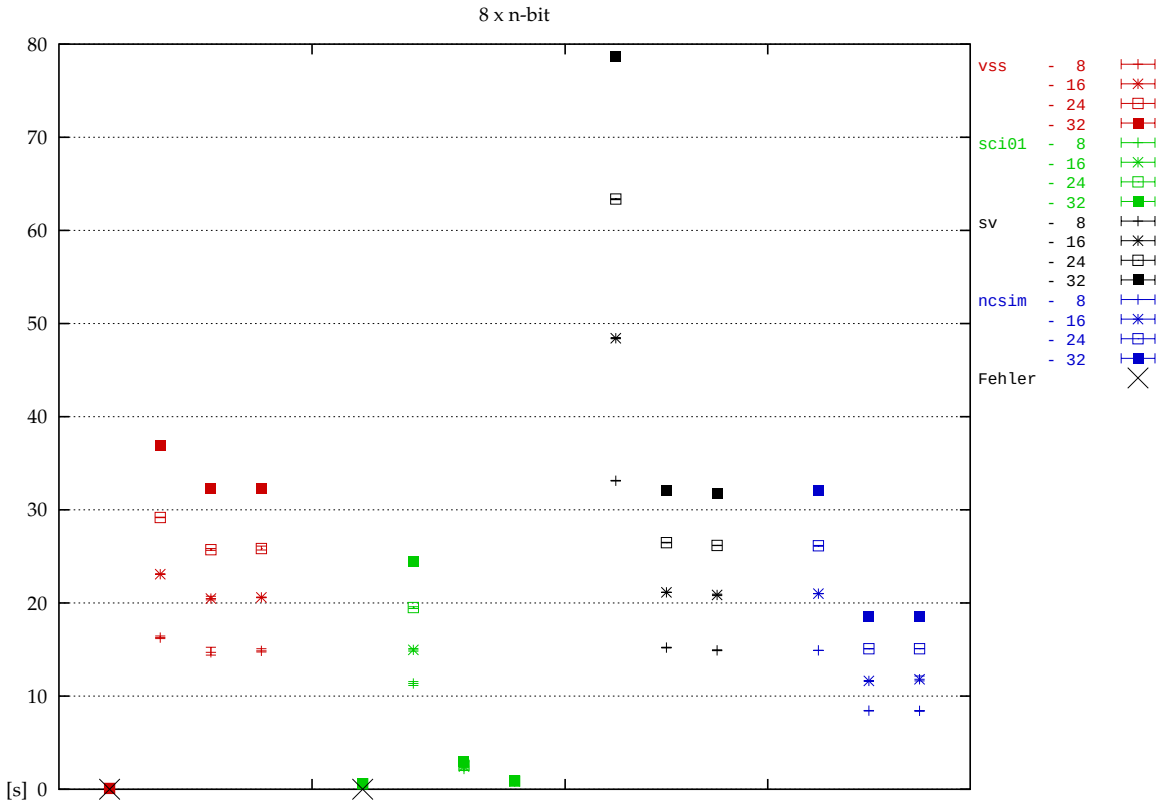
3.2 RT-Beschreibung, Referenz zur Netzliste

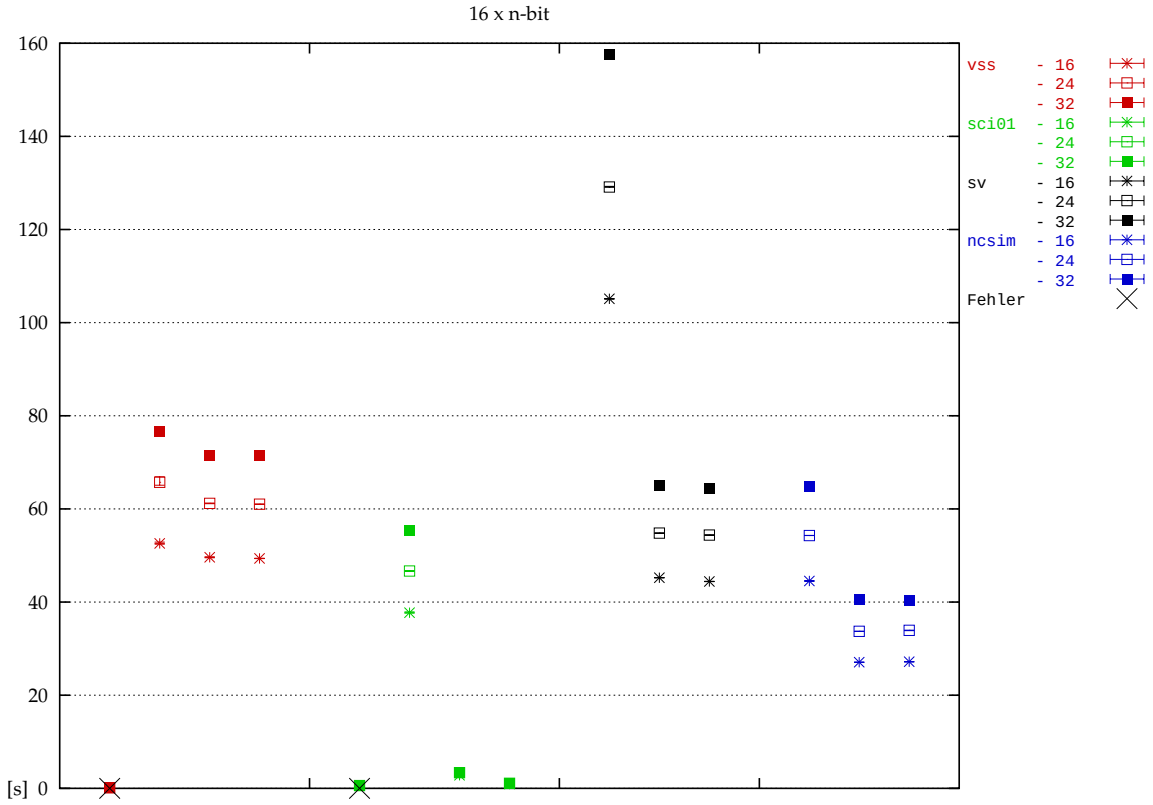
Tabelle 16: Booth-Multiplizierer, RT-Code, Referenz zur Netzliste

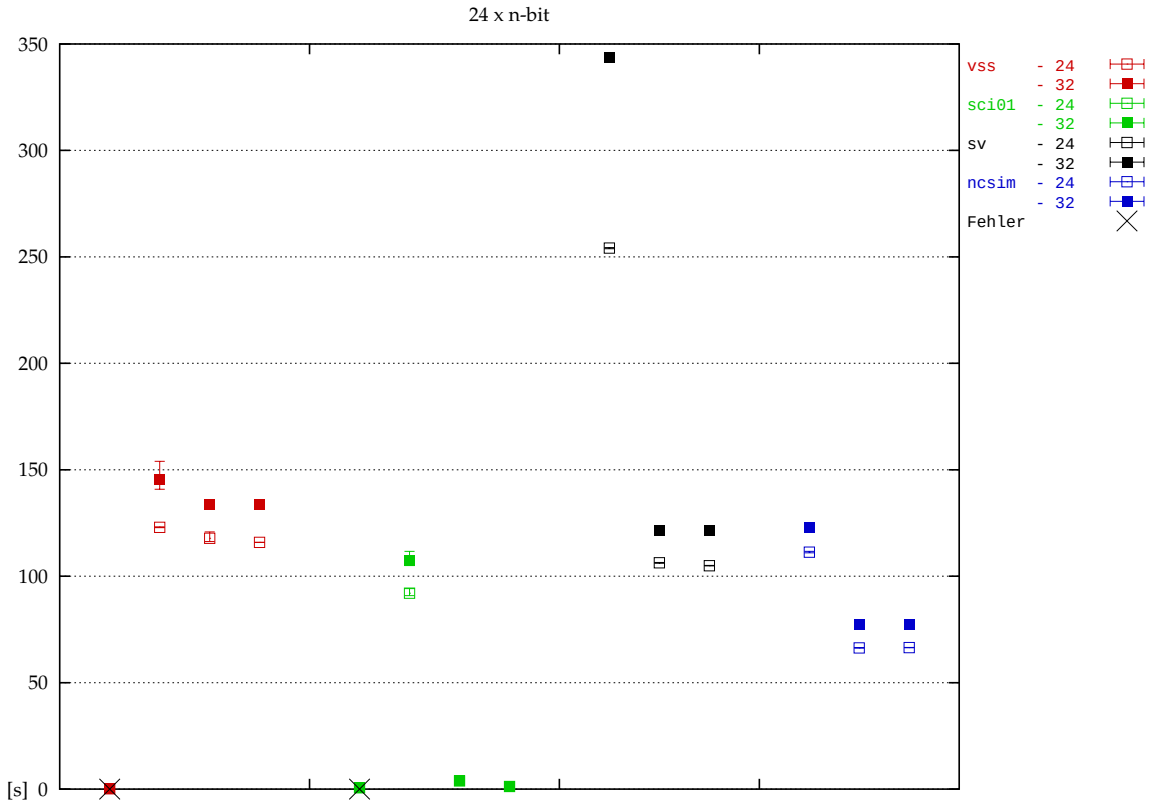
Register-Transfer Code					Referenzzyklen	
	× 8 bit	× 16 bit	× 24 bit	× 32 bit		
Simulator	avg. [s]	avg. [s]	avg. [s]	avg. [s]	Parameter	Fehler
VSS					vss.3	mul.1
8 × ...	16,27	23,09	29,18	36,9	vss.4	
	14,69	20,48	25,73	32,26	vss.5	
	14,86	20,6	25,85	32,31	vss.6	
16 × ...		52,6	65,73	76,7	vss.4	
		49,63	61,19	71,42	vss.5	
		49,36	61,02	71,54	vss.6	
24 × ...			122,98	145,43	vss.4	
			117,78	133,55	vss.5	
			115,89	133,74	vss.6	
32 × ...				219,76	vss.4	
				208,63	vss.5	
				211,3	vss.6	
Scirocco '01					scs.1	mul.1
8 × ...	11,36	14,96	19,5	24,47	scs.2	
	2,17	2,44	2,57	2,95	scs.3	
	0,85	0,85	0,88	0,91	scs.4	
16 × ...		37,7	46,68	55,42	scs.2	
		2,82	3,36	3,47	scs.3	
		0,9	1,1	1,07	scs.4	
24 × ...			92,01	107,31	scs.2	
			3,81	4,03	scs.3	
			1,24	1,24	scs.4	
32 × ...				168,13	scs.2	
				4,52	scs.3	
				1,43	scs.4	
Leapfrog	33,13	48,42	63,37	78,72	lea.1	
8 × ...	15,21	21,14	26,48	32,06	lea.2	
	14,91	20,86	26,18	31,76	lea.3	
16 × ...		105,13	129,14	157,53	lea.1	
		45,22	54,8	64,97	lea.2	
		44,42	54,39	64,45	lea.3	
24 × ...			254,1	343,44	lea.1	
			106,28	121,62	lea.2	
			104,93	121,63	lea.3	
32 × ...				542,35	lea.1	
				190,23	lea.2	
				189,69	lea.3	

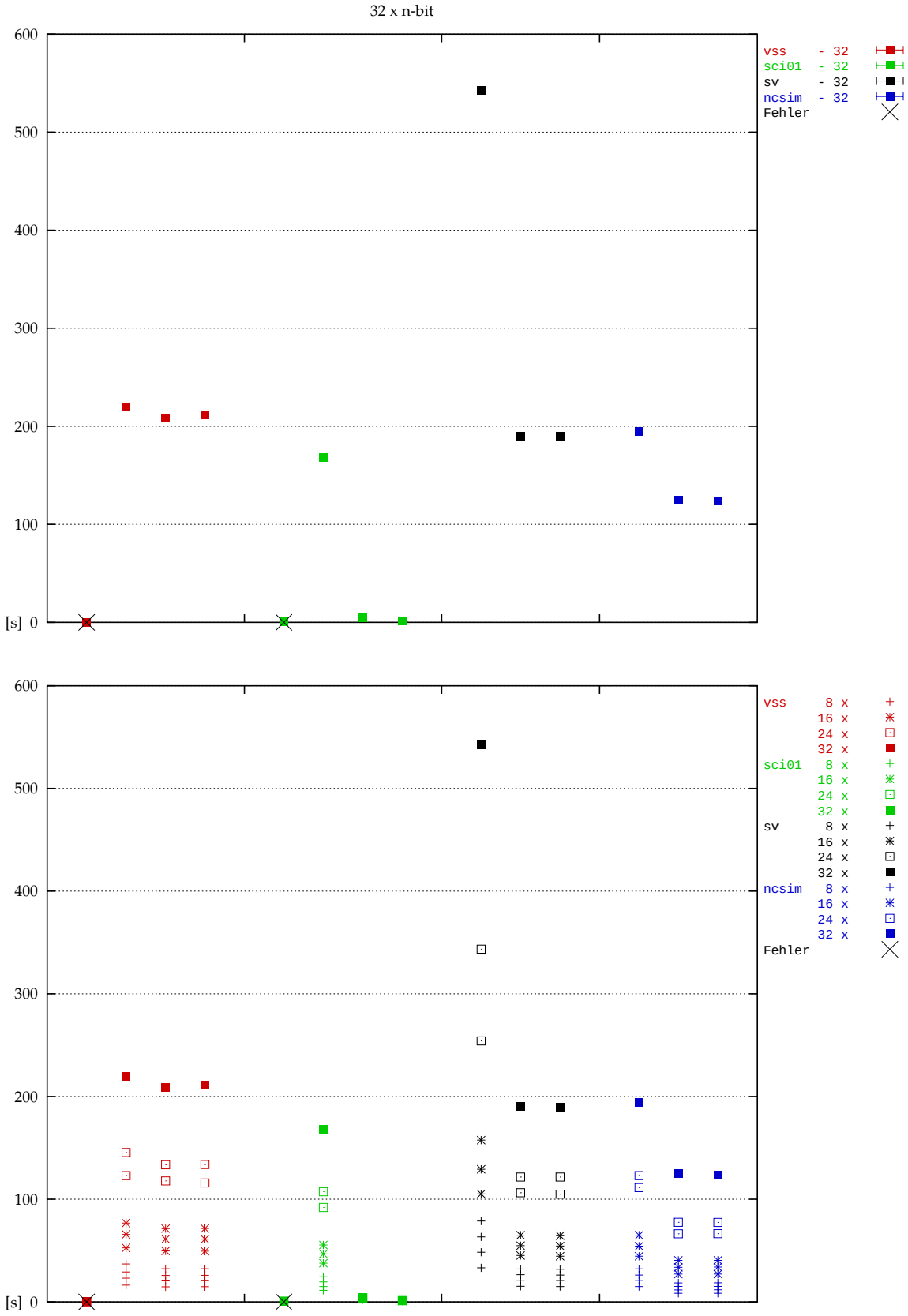
nächste Seite

Register-Transfer Code					Referenzzyklen	
Simulator	× 8 bit avg. [s]	× 16 bit avg. [s]	× 24 bit avg. [s]	× 32 bit avg. [s]	Parameter	Fehler
NCSim	14,91	21,0	26,13	32,12	ncs.1	
8 × ...	8,43	11,62	15,09	18,52	ncs.2	
	8,41	11,8	15,09	18,54	ncs.3	
16 × ...		44,53	54,3	64,91	ncs.1	
		27,08	33,73	40,45	ncs.2	
		27,19	33,91	40,41	ncs.3	
24 × ...			111,3	123,01	ncs.1	
			66,35	77,51	ncs.2	
			66,44	77,33	ncs.3	
32 × ...				194,47	ncs.1	
				124,7	ncs.2	
				123,71	ncs.3	




16 x n-bit
160
140
120
100
80
60
40
20
[s] 0
vss - 16
- 24
- 32
sci01 - 16
- 24
- 32
sv - 16
- 24
- 32
ncsim - 16
- 24
- 32
Fehler


24 x n-bit
350
300
250
200
150
100
50
[s] 0
vss - 24
- 32
sci01 - 24
- 32
sv - 24
- 32
ncsim - 24
- 32
Fehler


32 x n-bit
600
500
400
300
200
100
[s] 0
vss - 32
sci01 - 32
sv - 32
ncsim - 32
Fehler
vss 8 x
16 x
24 x
32 x
sci01 8 x
16 x
24 x
32 x
sv 8 x
16 x
24 x
32 x
ncsim 8 x
16 x
24 x
32 x
Fehler

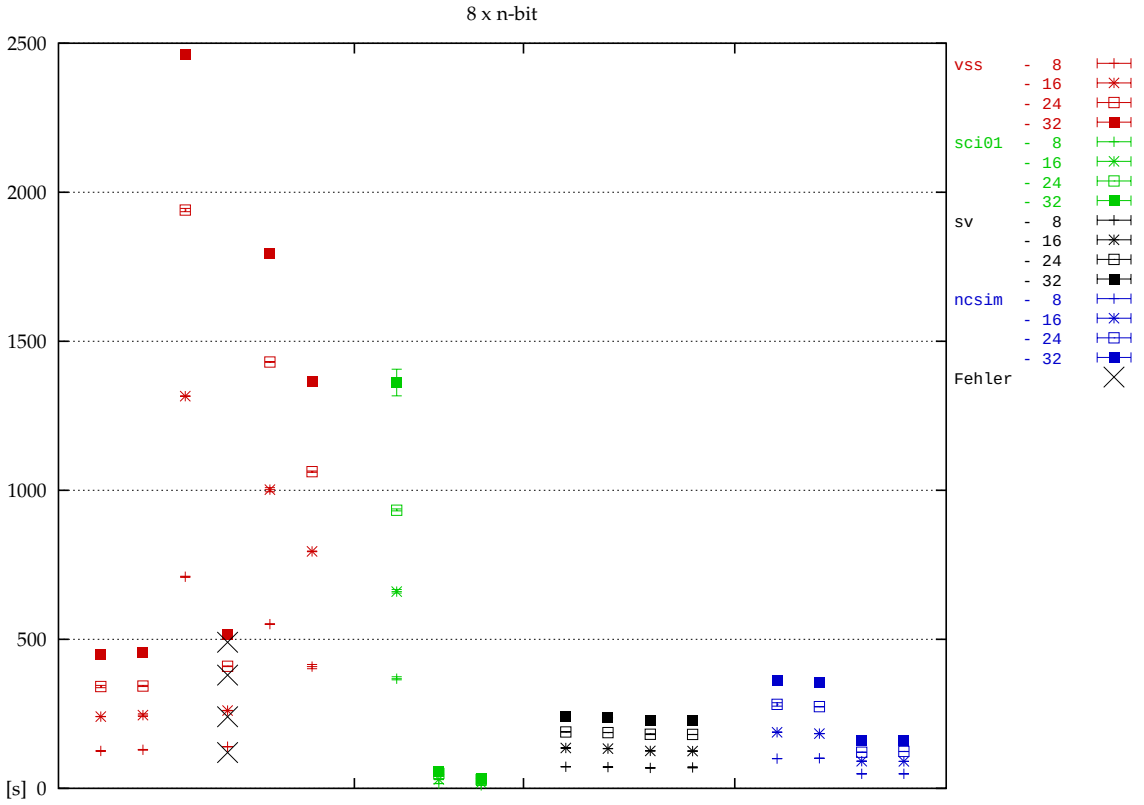
3.3 Netzliste, VHDL Simulation

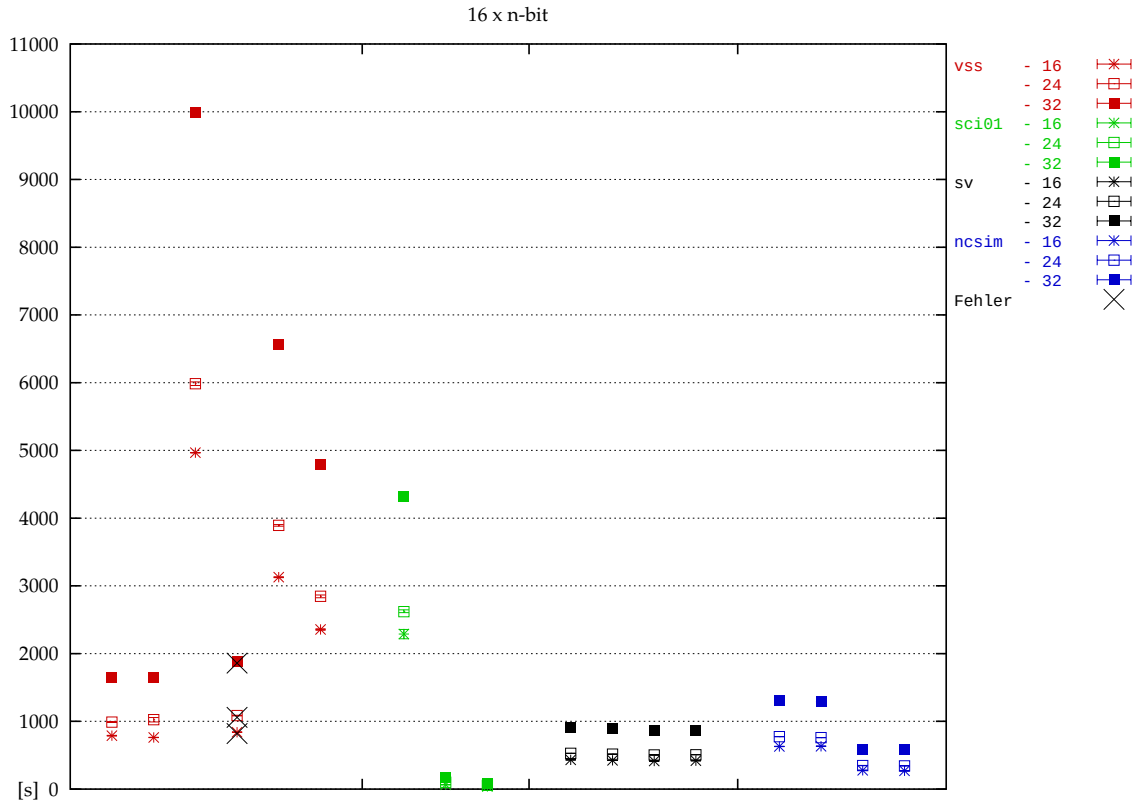
Tabelle 17: Booth-Multiplizierer, AMS-Netzliste

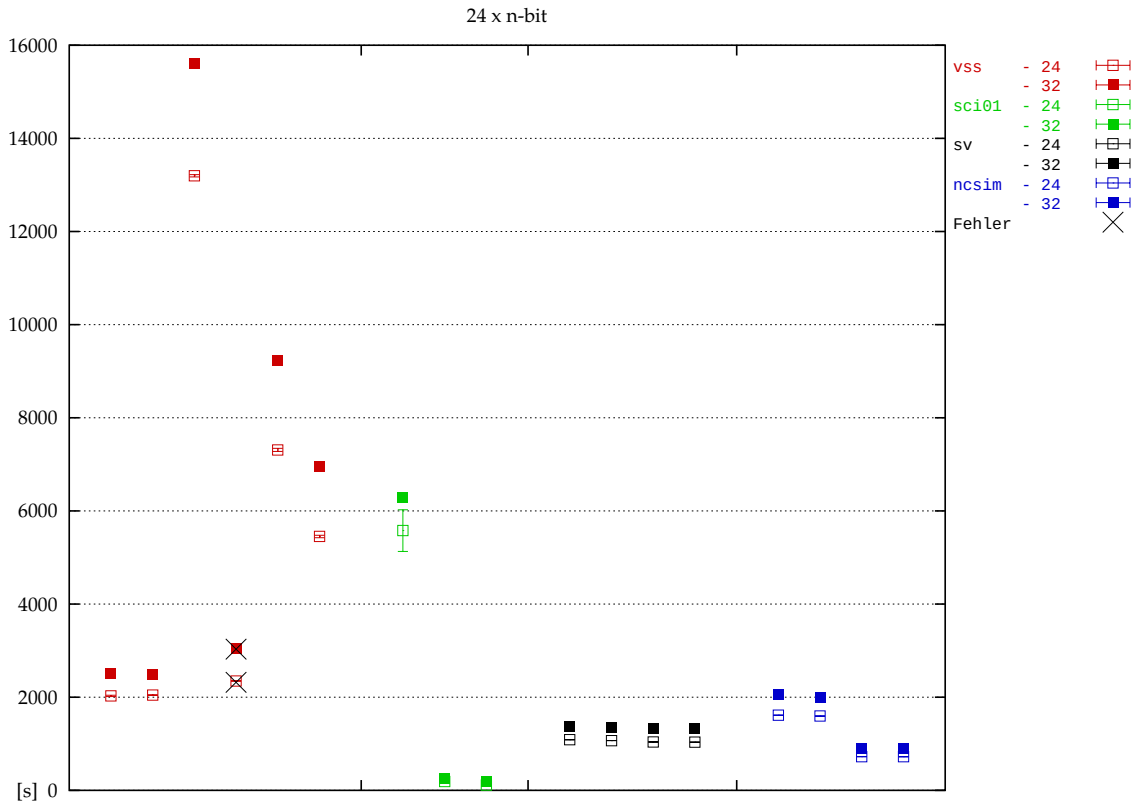
Netzliste – VHDL					AMS-Prozess	
	× 8 bit	× 16 bit	× 24 bit	× 32 bit		
Simulator	avg. [s]	avg. [s]	avg. [s]	avg. [s]	Parameter	Fehler
VSS	125,32	240,79	341,67	448,71	vss.6	FTGS
8 × ...	129,24	245,83	343,37	454,46	vss.6	FTGSC
	709,83	1315,77	1940,19	2460,27	vss.6	FTSM
	139,87	261,08	409,76	516,07	vss.6	UDSM mul.2
	550,84	1001,96	1430,61	1795,47	vss.6	VITAL
	408,65	794,97	1062,54	1364,49	vss.6	vital
16 × ...		788,15	989,97	1655,3	vss.6	FTGS
		761,97	1024,72	1640,05	vss.6	FTGSC
		4966,38	5984,67	9991,06	vss.6	FTSM
		840,67	1084,99	1881,05	vss.6	UDSM mul.2
		3128,08	3892,7	6559,99	vss.6	VITAL
		2355,97	2846,1	4791,31	vss.6	vital
24 × ...			2027,11	2505,04	vss.6	FTGS
			2045,36	2484,38	vss.6	FTGSC
			13196,37	15618,53	vss.6	FTSM
			2348,01	3054,35	vss.6	UDSM mul.2
			7310,35	9219,58	vss.6	VITAL
			5450,9	6954,78	vss.6	vital
32 × ...				3802,83	vss.6	FTGS
				3744,86	vss.6	FTGSC
				24078,96	vss.6	FTSM
				4682,61	vss.6	UDSM mul.2
				12859,42	vss.6	VITAL
				10057,02	vss.6	vital
Scirocco '01	367,99	660,03	933,19	1361,67	scs.2	
8 × ...	16,12	29,99	49,94	57,58	scs.3	
	9,82	18,11	29,7	34,59	scs.4	
16 × ...		2290,04	2619,26	4322,63	scs.2	
		65,93	102,04	162,99	scs.3	
		38,91	55,73	80,72	scs.4	
24 × ...			5577,74	6296,12	scs.2	
			189,78	255,97	scs.3	
			110,69	184,23	scs.4	
32 × ...				9289,79	scs.2	
				438,62	scs.3	
				211,32	scs.4	

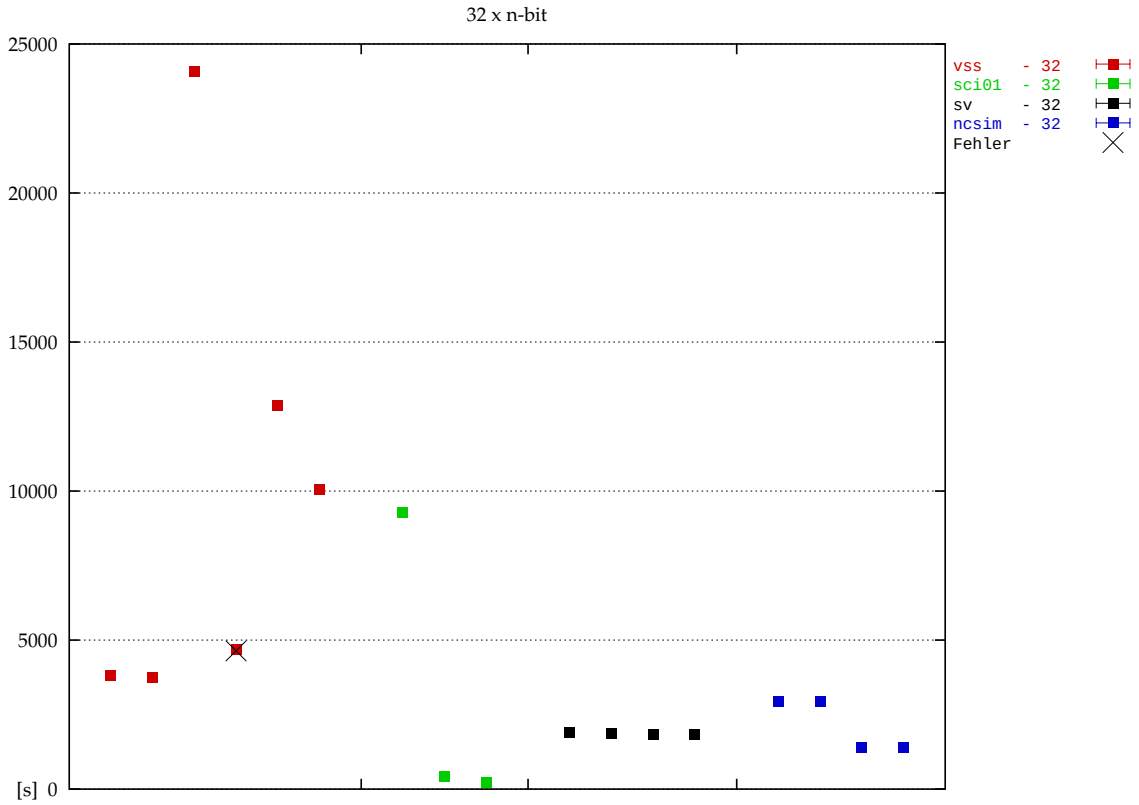
nächste Seite

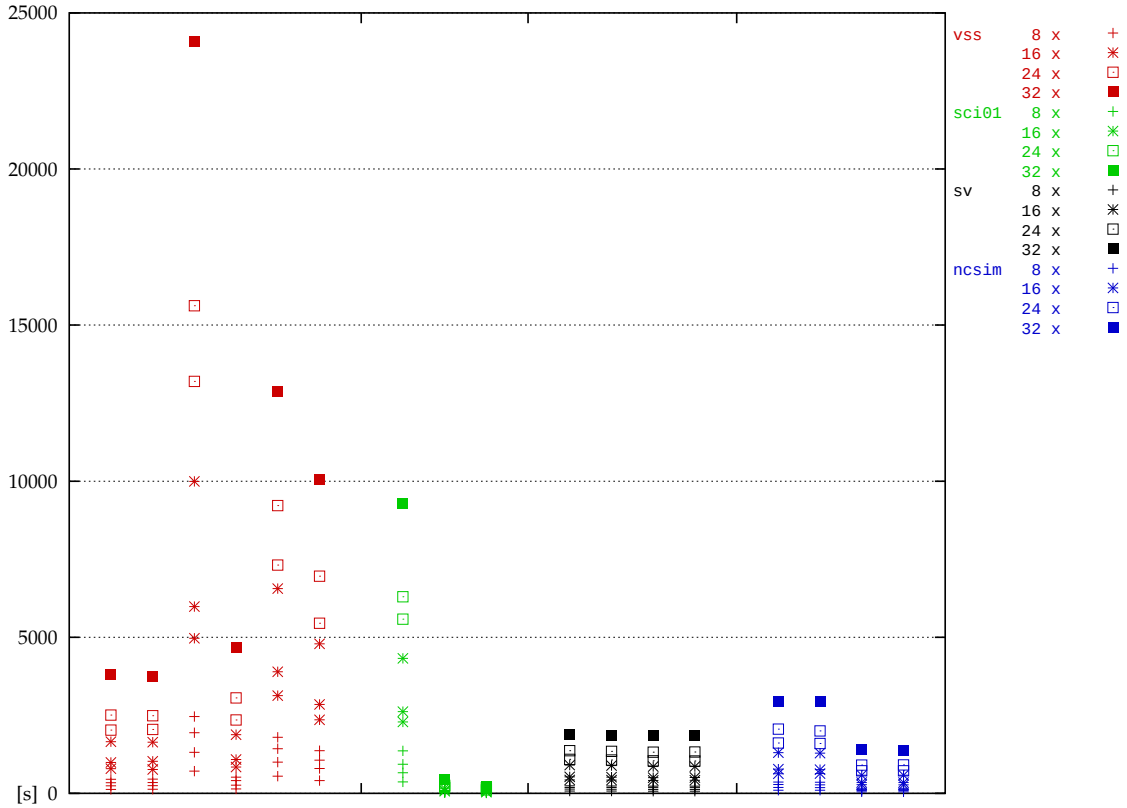
Netzliste – VHDL					AMS-Prozess	
	× 8 bit	× 16 bit	× 24 bit	× 32 bit		
Simulator	avg. [s]	avg. [s]	avg. [s]	avg. [s]	Parameter	Fehler
Leapfrog	72,52	135,4	189,37	239,98	lea.2	
8 × ...	71,45	133,38	187,09	236,35	lea.3	
	68,68	125,72	181,71	228,97	lea.2 opt	
	70,43	125,04	180,78	228,72	lea.3 opt	
16 × ...		430,68	527,35	903,73	lea.2	
		423,47	516,94	891,99	lea.3	
		415,42	504,33	857,98	lea.2 opt	
		420,7	507,34	859,65	lea.3 opt	
24 × ...			1087,16	1364,64	lea.2	
			1068,15	1346,39	lea.3	
			1039,46	1320,33	lea.2 opt	
			1034,61	1324,83	lea.3 opt	
32 × ...				1890,13	lea.2	
				1858,41	lea.3	
				1842,28	lea.2 opt	
				1838,05	lea.3 opt	
NCSim	99,88	188,12	281,56	362,83	ncs.2 vhdl	
8 × ...	100,75	183,84	273,9	355,27	ncs.3 vhdl	
	48,82	90,87	121,25	160,34	ncs.2 vlog	
	48,88	90,67	123,7	160,67	ncs.3 vlog	
16 × ...		629,14	774,77	1304,13	ncs.2 vhdl	
		632,97	759,66	1289,9	ncs.3 vhdl	
		276,79	346,99	580,65	ncs.2 vlog	
		270,73	343,69	581,48	ncs.3 vlog	
24 × ...			1614,04	2055,07	ncs.2 vhdl	
			1595,39	2000,93	ncs.3 vhdl	
			723,98	904,64	ncs.2 vlog	
			721,91	909,78	ncs.3 vlog	
32 × ...				2944,13	ncs.2 vhdl	
				2932,75	ncs.3 vhdl	
				1401,38	ncs.2 vlog	
				1382,35	ncs.3 vlog	

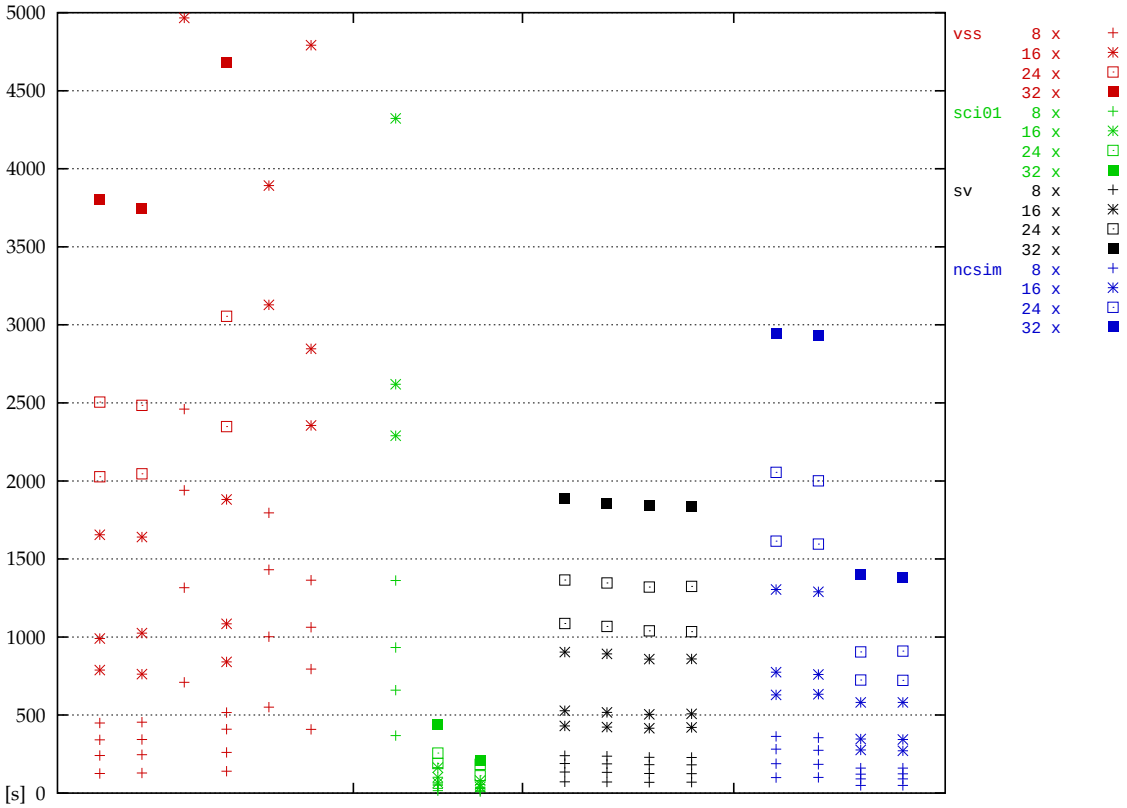

8 x n-bit
2500
2000
1500
1000
500
[s] 0
vss - 8
- 16
- 24
- 32
sci01 - 8
- 16
- 24
- 32
sv - 8
- 16
- 24
- 32
ncsim - 8
- 16
- 24
- 32
Fehler

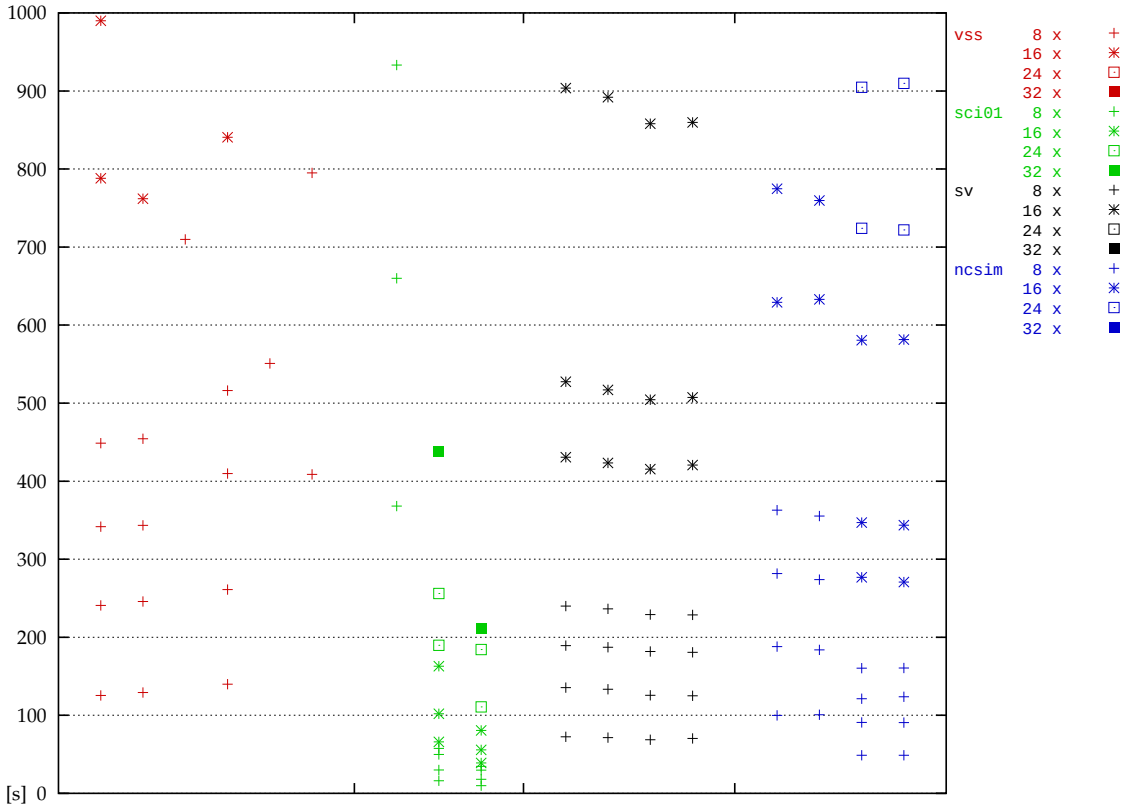

16 x n-bit
11000
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
[s] 0
vss - 16
- 24
- 32
sci01 - 16
- 24
- 32
sv - 16
- 24
- 32
ncsim - 16
- 24
- 32
Fehler


24 x n-bit
16000
14000
12000
10000
8000
6000
4000
2000
[s] 0
vss - 24
- 32
sci01 - 24
- 32
sv - 24
- 32
ncsim - 24
- 32
Fehler


32 x n-bit
25000
20000
15000
10000
5000
[s] 0
vss - 32
sci01 - 32
sv - 32
ncsim - 32
Fehler


25000
20000
15000
10000
5000
[s] 0
vss 8 x
16 x
24 x
32 x
sci01 8 x
16 x
24 x
32 x
sv 8 x
16 x
24 x
32 x
ncsim 8 x
16 x
24 x
32 x


5000
4500
4000
3500
3000
2500
2000
1500
1000
500
[s] 0
vss 8 x
16 x
24 x
32 x
sci01 8 x
16 x
24 x
32 x
sv 8 x
16 x
24 x
32 x
ncsim 8 x
16 x
24 x
32 x



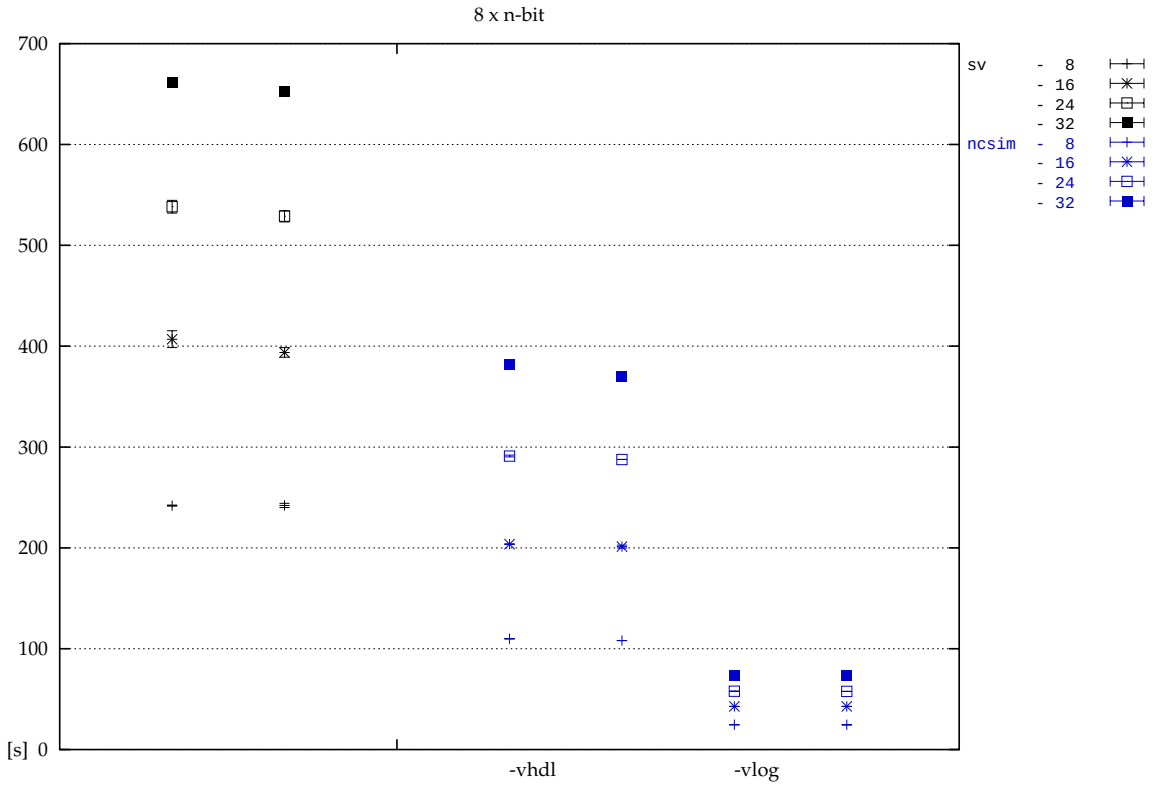
3.4 Netzliste, mixed-mode Simulation

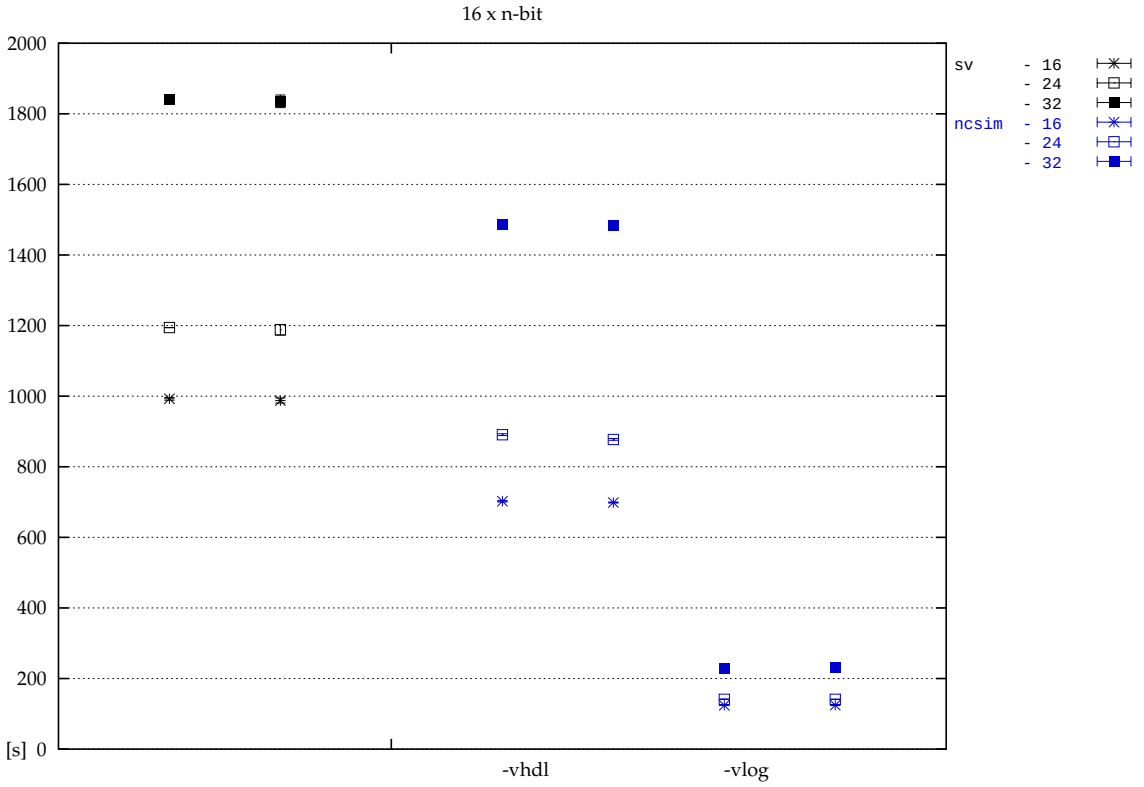
Tabelle 18: Booth-Multiplizierer, AMS-Netzliste, mixed-mode Simulation

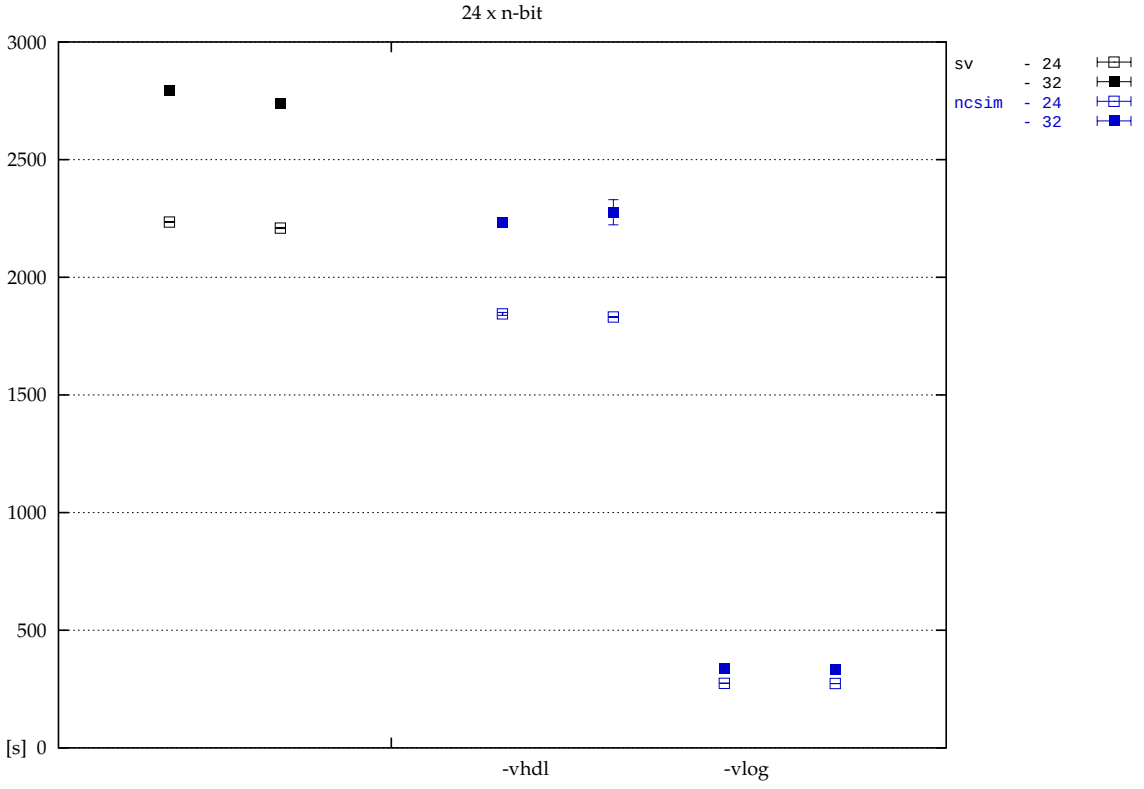
Netzliste – VHDL + Verilog					AMS-Prozess	
Simulator	× 8 bit avg. [s]	× 16 bit avg. [s]	× 24 bit avg. [s]	× 32 bit avg. [s]	Parameter	Fehler
Leapfrog	241,95	406,92	538,3	661,44	lem.1	
8 × ...	242,06	393,83	528,86	652,84	lem.2	
16 × ...		992,38	1194,25	1841,19	lem.1	
		987,71	1188,14	1835,33	lem.2	
24 × ...			2234,97	2793,74	lem.1	
			2209,32	2739,66	lem.2	
32 × ...				3946,75	lem.1	
				3935,62	lem.2	
NCSim	109,89	203,68	291,09	382,21	ncm.1 vhdl	
8 × ...	108,03	201,27	287,7	369,79	ncm.2 vhdl	
	24,6	42,76	57,9	73,06	ncm.1 vlog	
	24,57	42,85	57,75	73,19	ncm.2 vlog	
16 × ...		702,31	890,82	1485,71	ncm.1 vhdl	
		698,51	877,41	1483,88	ncm.2 vhdl	
		124,28	141,41	229,72	ncm.1 vlog	
		124,64	141,36	230,02	ncm.2 vlog	
24 × ...			1844,53	2233,96	ncm.1 vhdl	

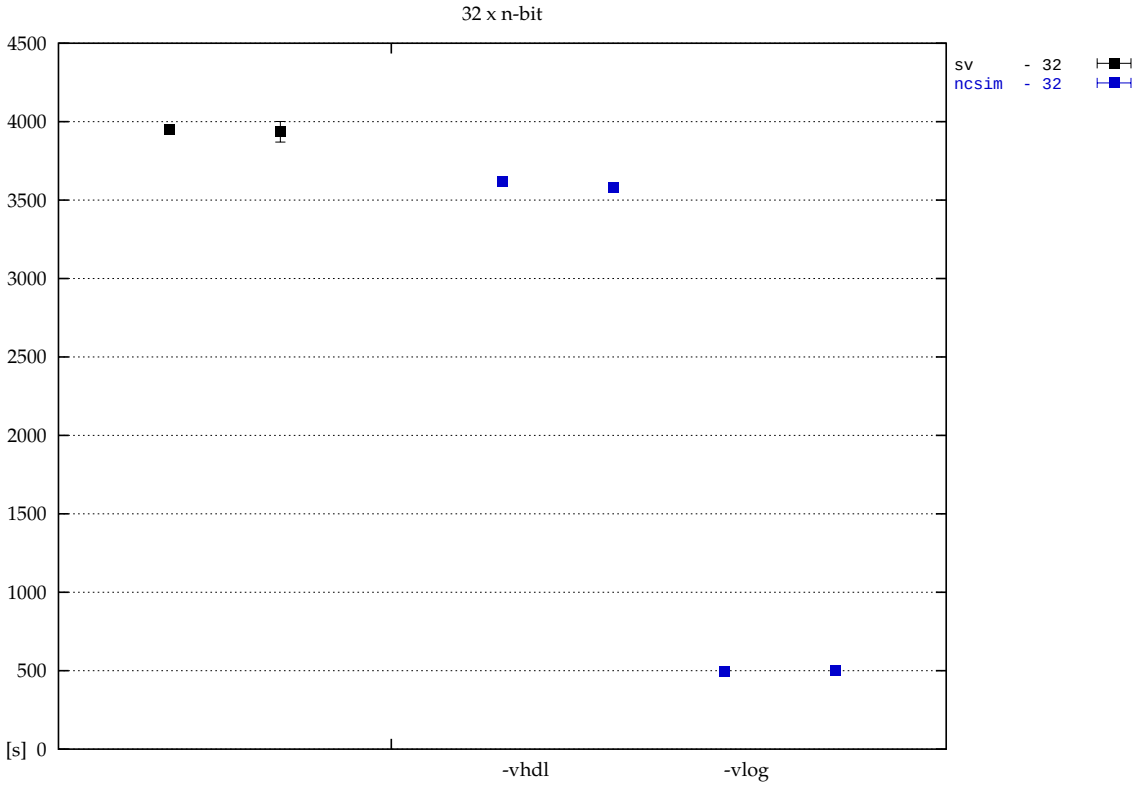
nächste Seite

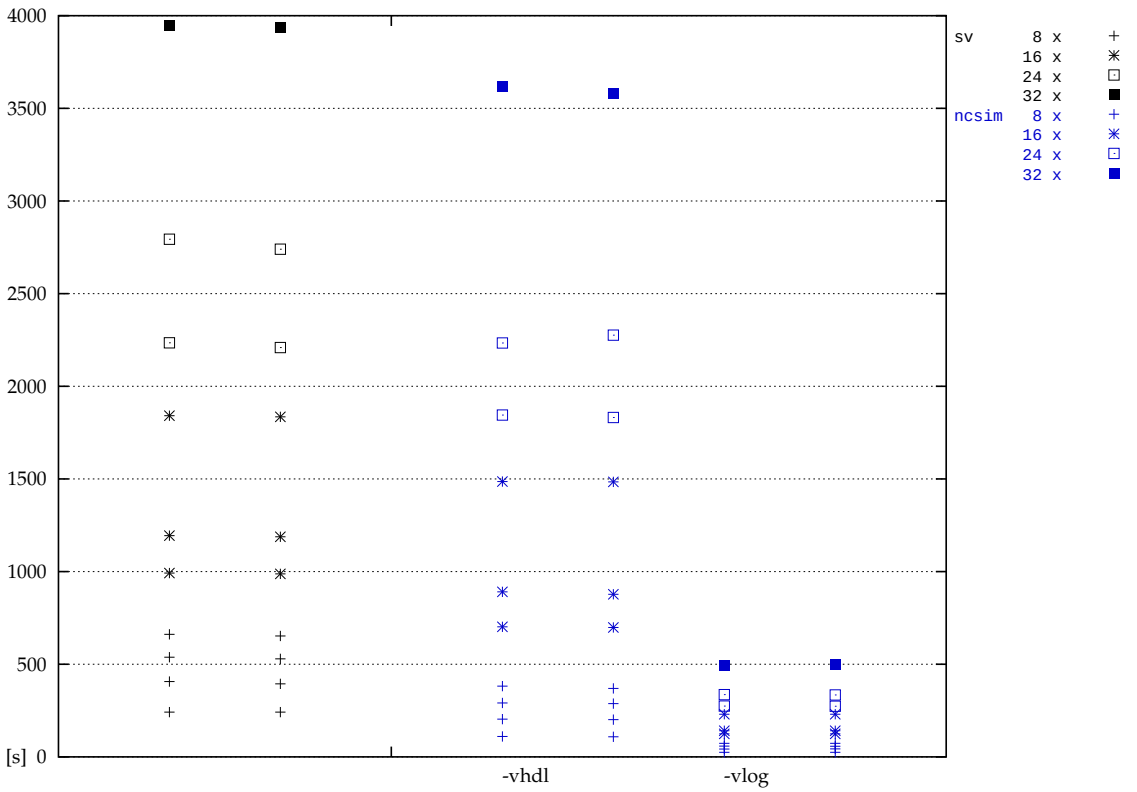
Netzliste – VHDL + Verilog					AMS-Prozess	
Simulator	× 8 bit avg. [s]	× 16 bit avg. [s]	× 24 bit avg. [s]	× 32 bit avg. [s]	Parameter	Fehler
			1831,3	2276,39	ncm.2 vhdl	
			274,63	336,23	ncm.1 vlog	
			273,56	334,56	ncm.2 vlog	
32 × ...				3617,36	ncm.1 vhdl	
				3580,54	ncm.2 vhdl	
				492,22	ncm.1 vlog	
				500,17	ncm.2 vlog	



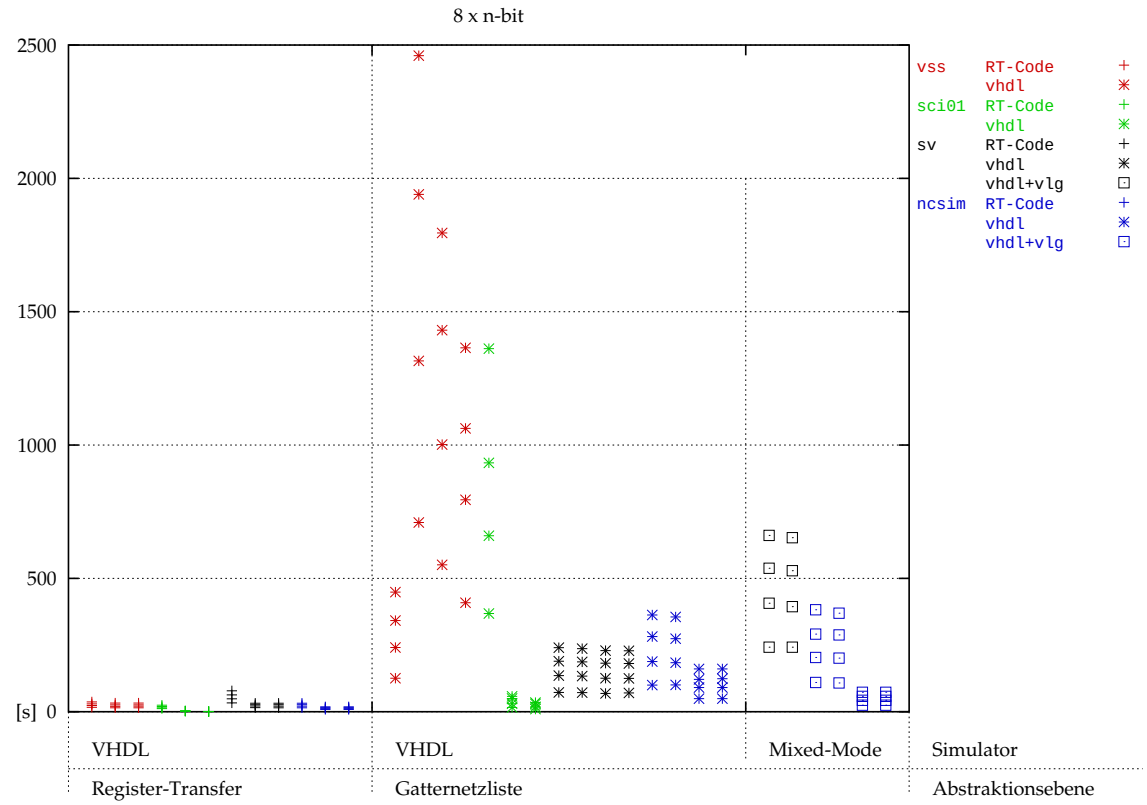

16 x n-bit
2000
1800
1600
1400
1200
1000
800
600
400
200
[s] 0
-vhdl
-vlog
sv - 16
- 24
- 32
ncsim - 16
- 24
- 32

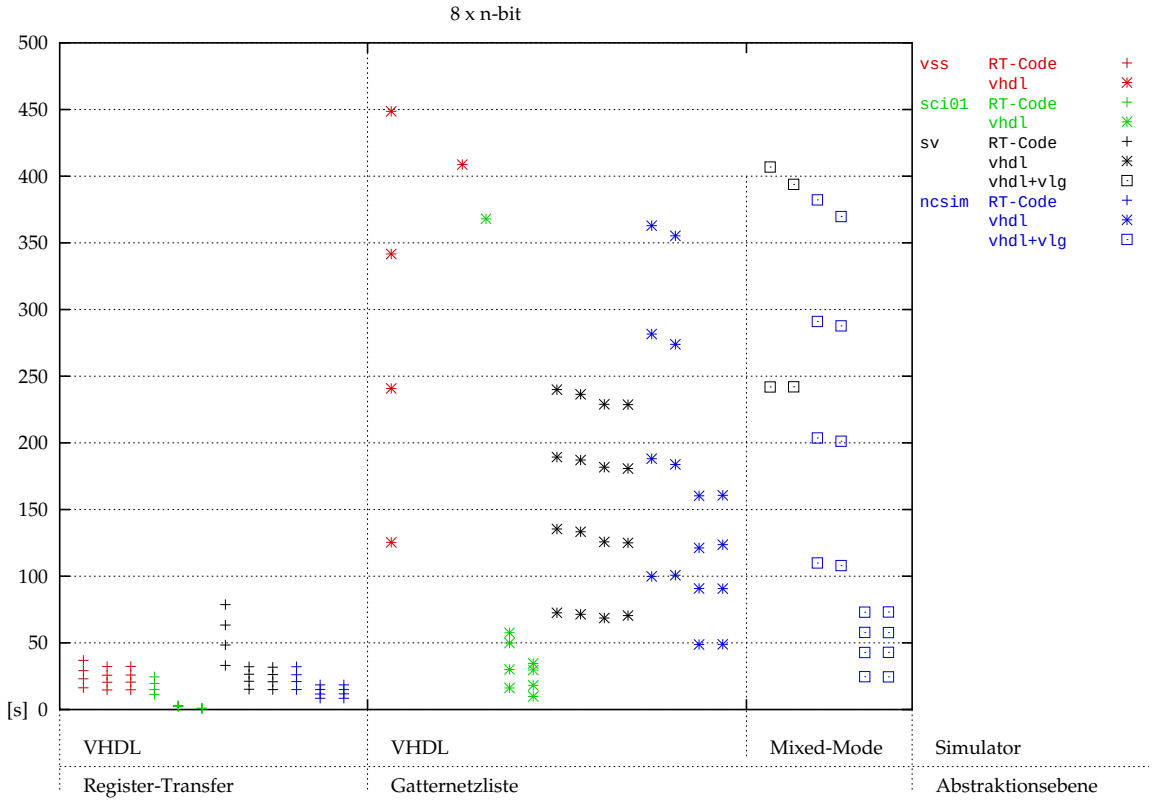

24 x n-bit
3000
2500
2000
1500
1000
500
[s] 0
-vhdl
-vlog
sv - 24
- 32
ncsim - 24
- 32

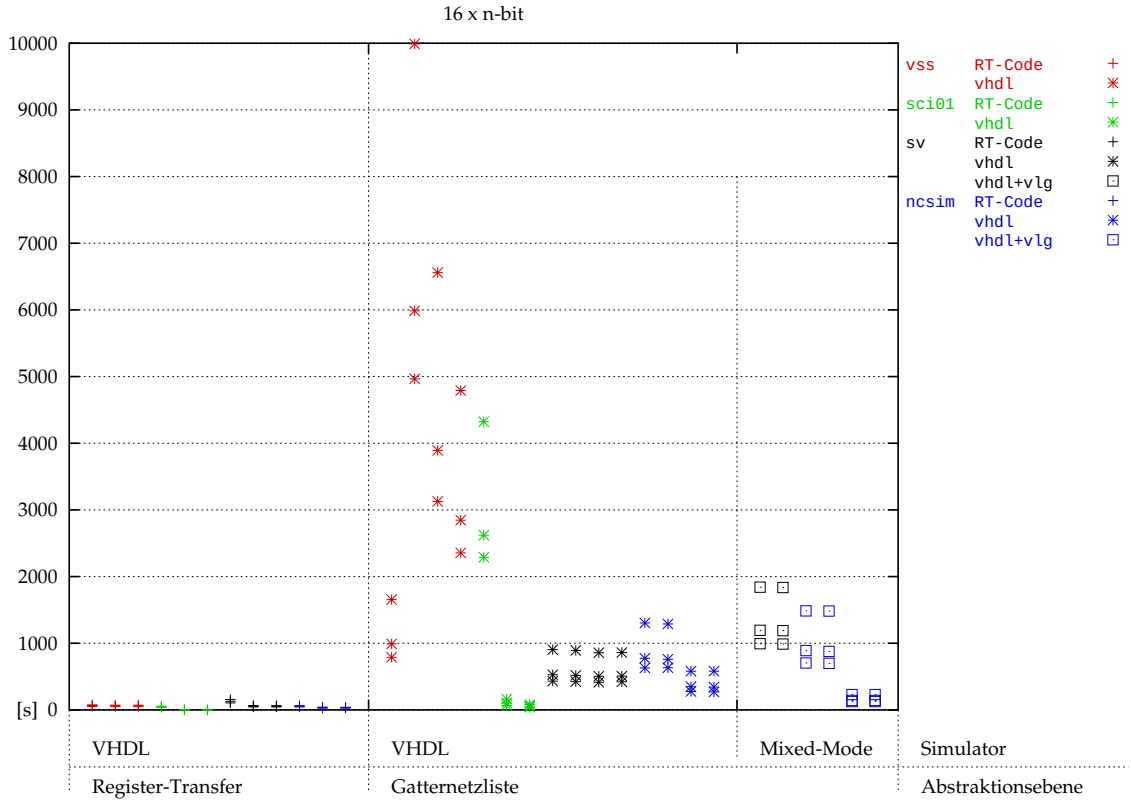

32 x n-bit
4500
4000
3500
3000
2500
2000
1500
1000
500
[s] 0
-vhdl
-vlog
sv - 32
ncsim - 32

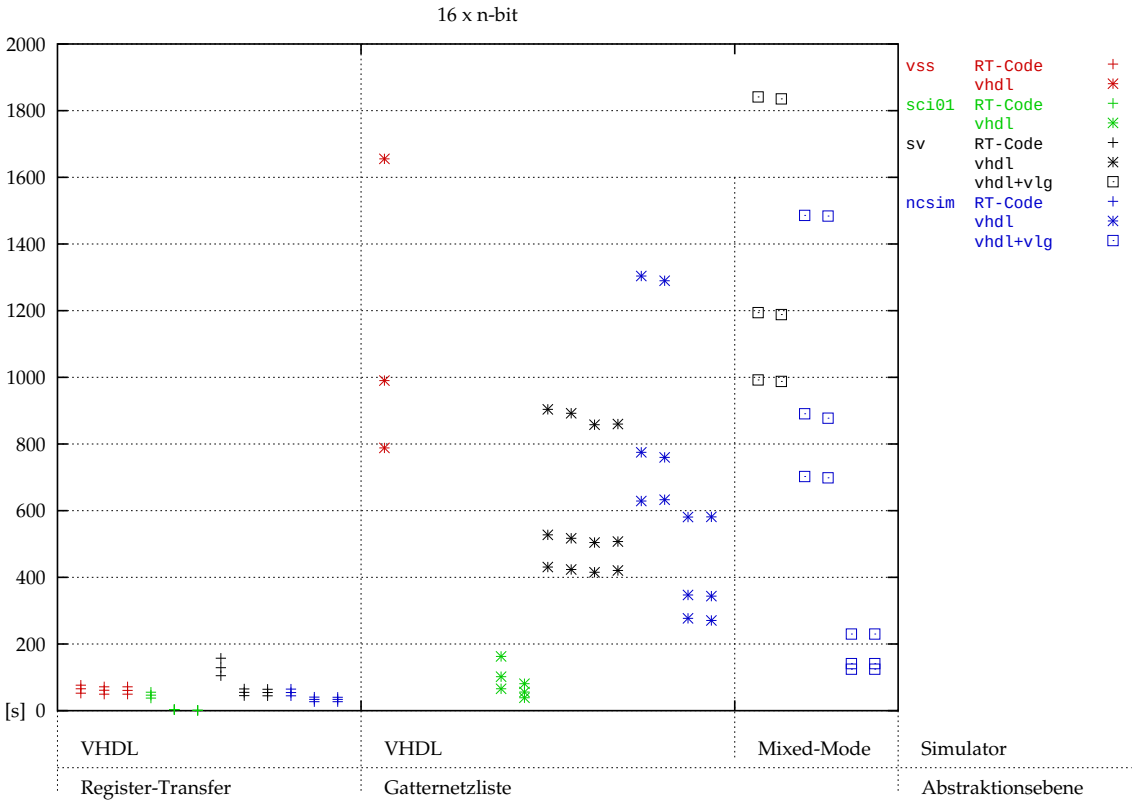

4000
3500
3000
2500
2000
1500
1000
500
[s] 0
-vhdl
-vlog
sv 8 x
16 x
24 x
32 x
ncsim 8 x
16 x
24 x
32 x

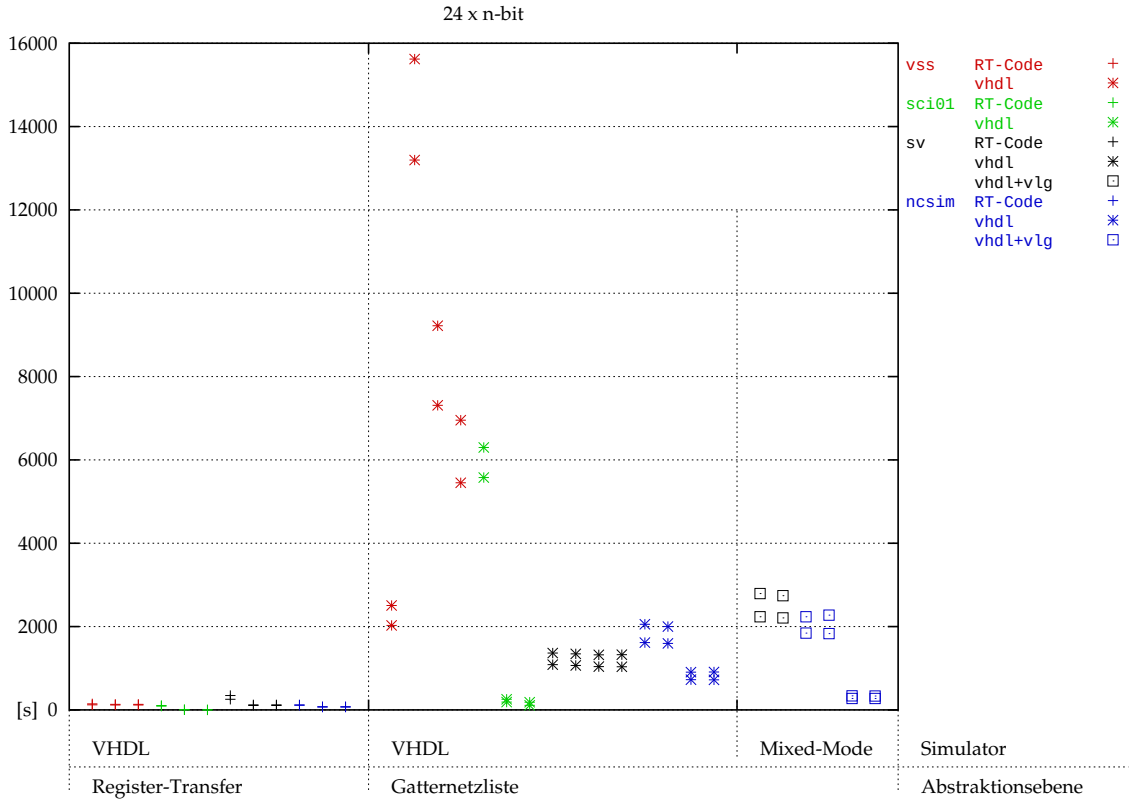
3.5 Übersicht

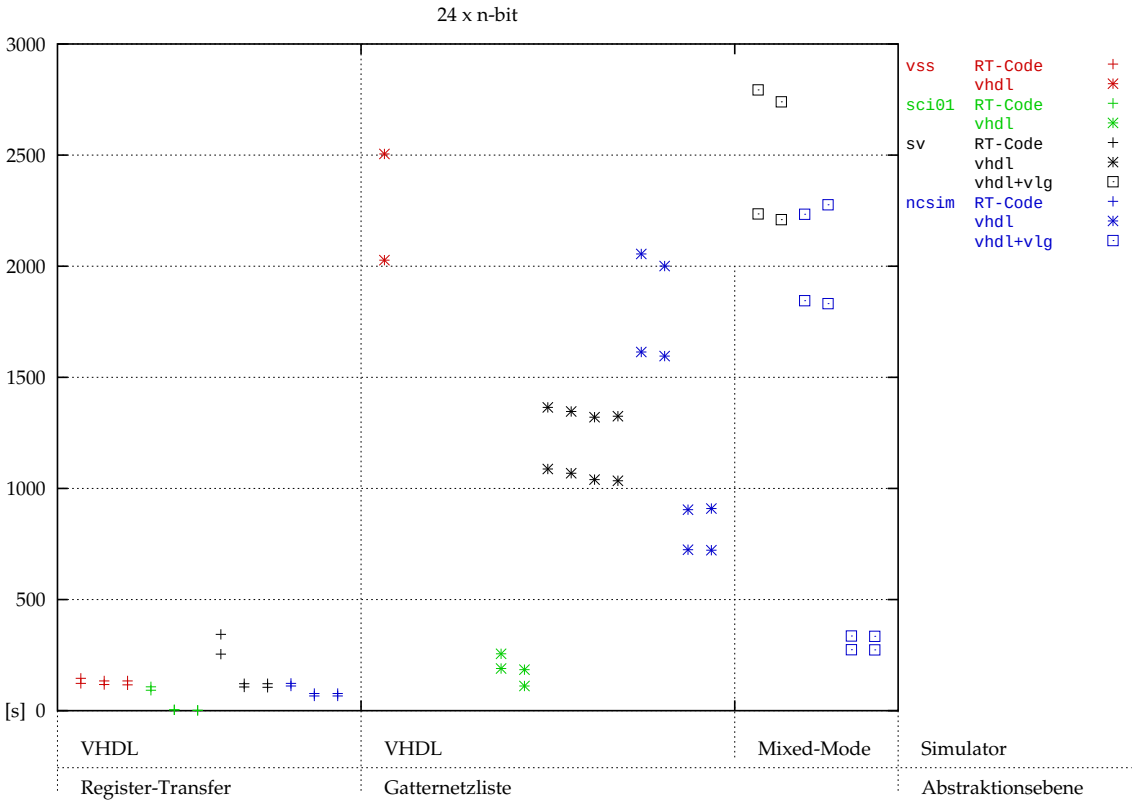


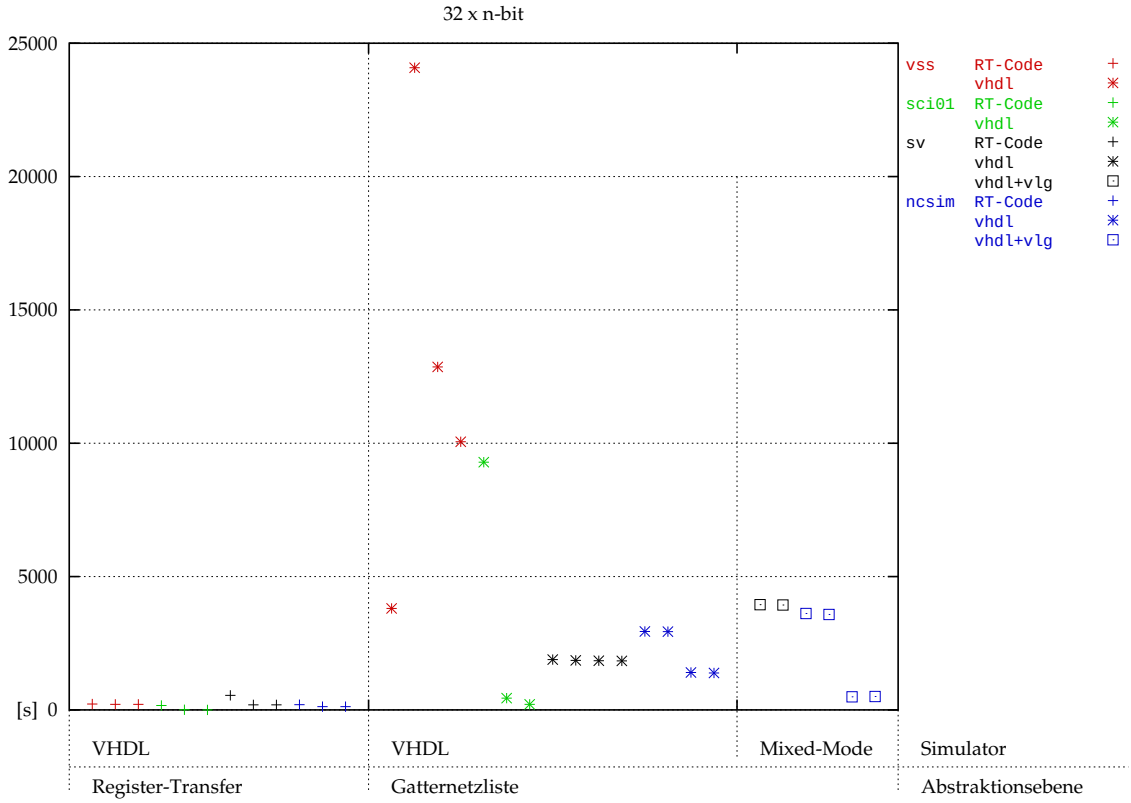


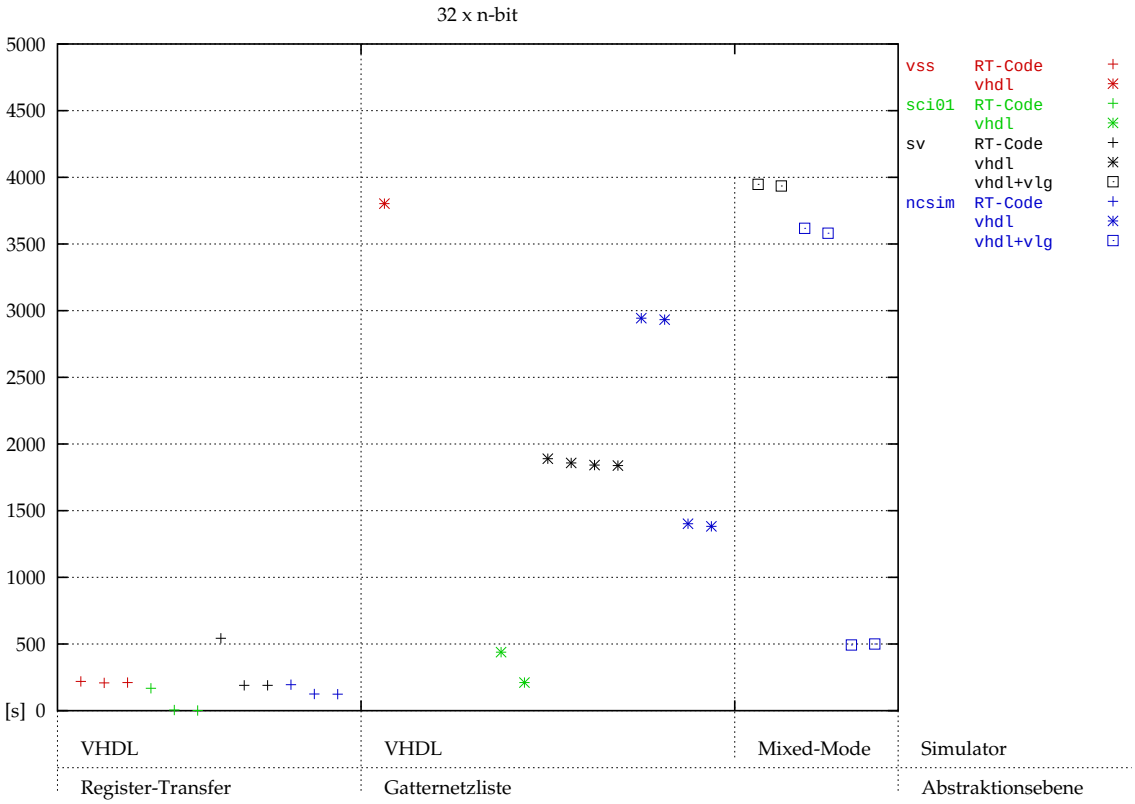

16 x n-bit
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
[s] 0
vss RT-Code
vhdl
sci01 RT-Code
vhdl
sv RT-Code
vhdl
vhdl+vlg
ncsim RT-Code
vhdl
vhdl+vlg
VHDL
Register-Transfer
VHDL
Gatternetzliste
Mixed-Mode
Simulator
Abstraktionsebene

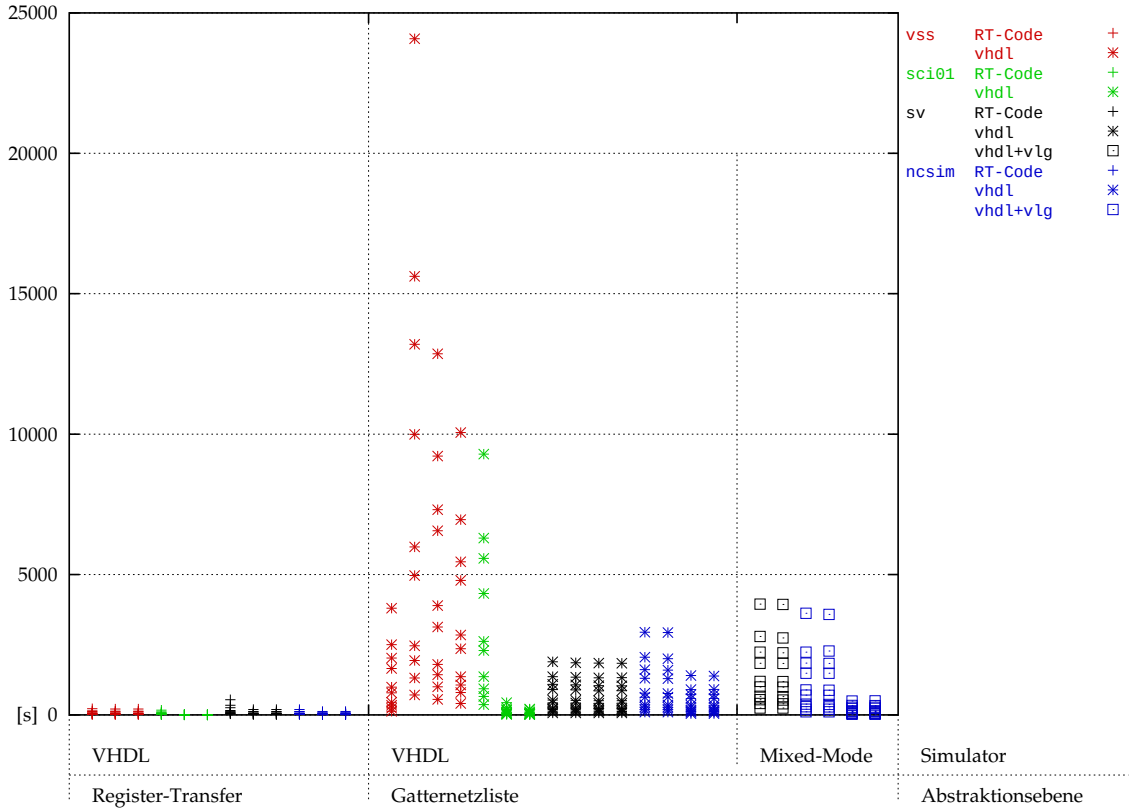

16 x n-bit
2000
1800
1600
1400
1200
1000
800
600
400
200
[s] 0
vss RT-Code
vhdl
sci01 RT-Code
vhdl
sv RT-Code
vhdl
vhdl+vlg
ncsim RT-Code
vhdl
vhdl+vlg
VHDL
Register-Transfer
VHDL
Gatternetzliste
Mixed-Mode
Simulator
Abstraktionsebene

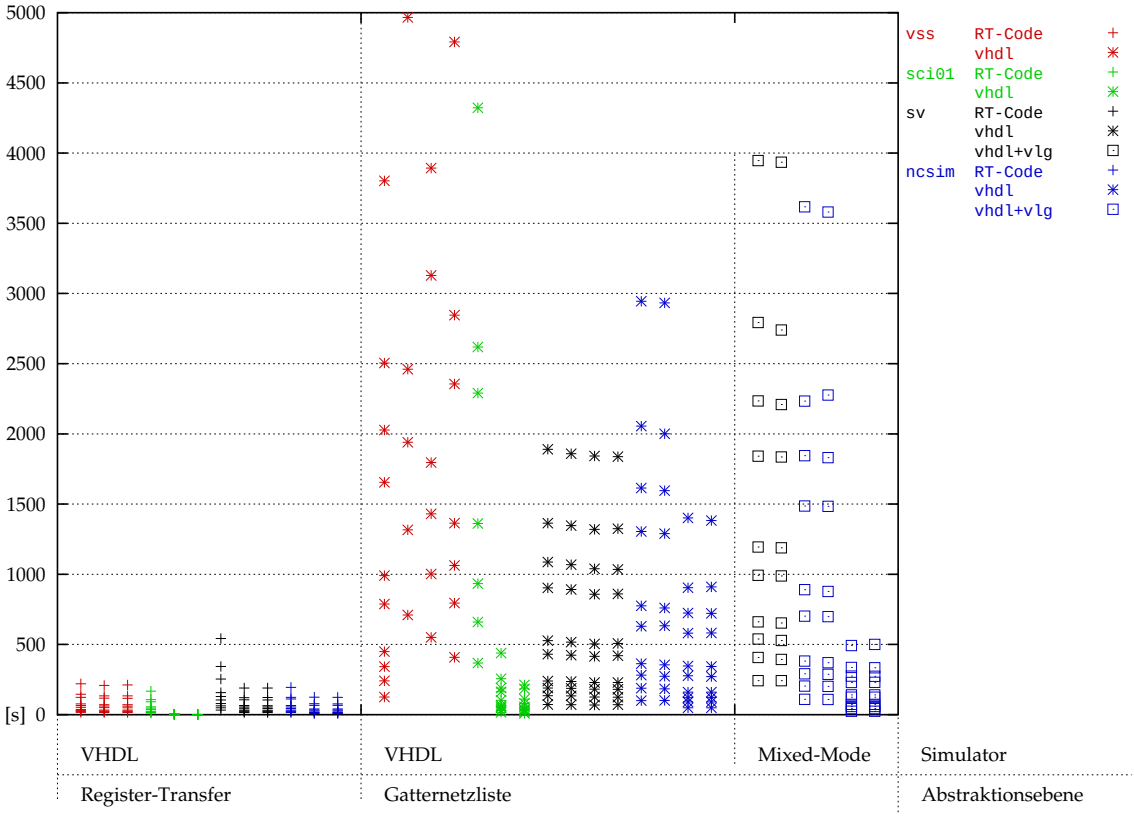

24 x n-bit
16000
14000
12000
10000
8000
6000
4000
2000
[s] 0
vss RT-Code
vhdl
sci01 RT-Code
vhdl
sv RT-Code
vhdl
vhdl+vlg
ncsim RT-Code
vhdl
vhdl+vlg
VHDL
Register-Transfer
VHDL
Gatternetzliste
Mixed-Mode
Simulator
Abstraktionsebene

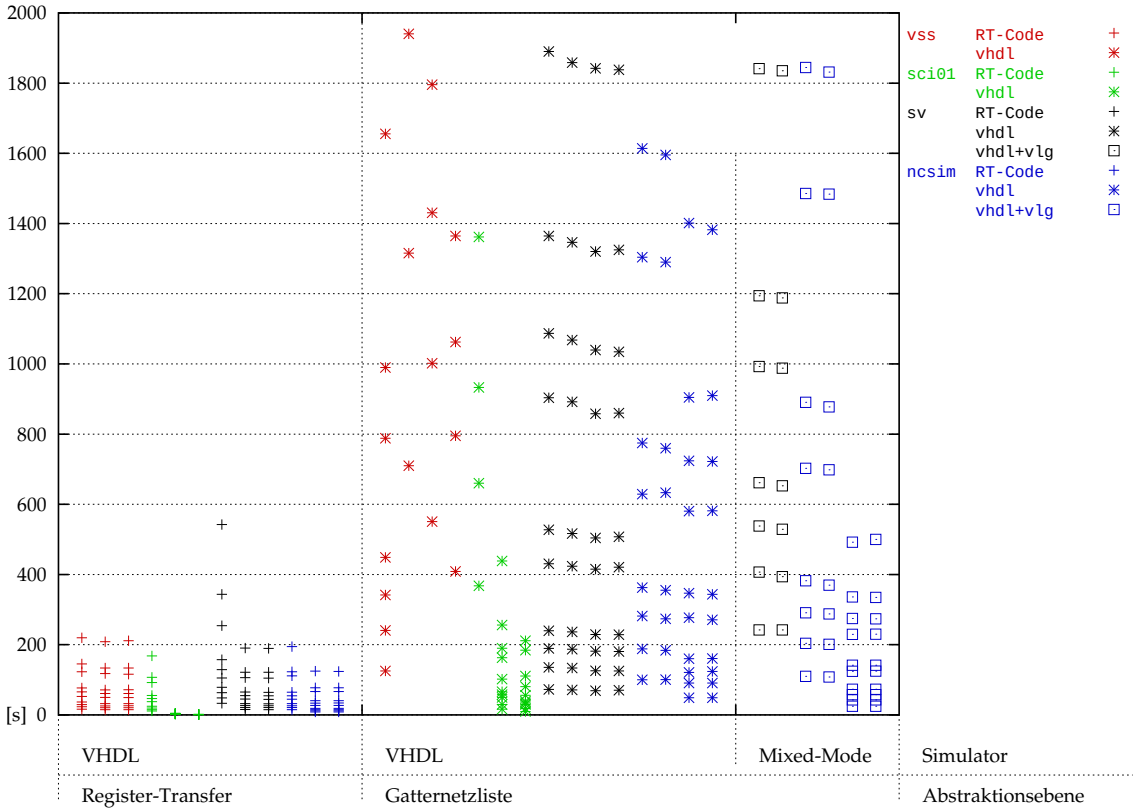

24 x n-bit
3000
2500
2000
1500
1000
500
[s] 0
vss RT-Code
vhdl
sci01 RT-Code
vhdl
sv RT-Code
vhdl
vhdl+vlg
ncsim RT-Code
vhdl
vhdl+vlg
VHDL
Register-Transfer
VHDL
Gatternetzliste
Mixed-Mode
Simulator
Abstraktionsebene


32 x n-bit
25000
20000
15000
10000
5000
[s] 0
vss RT-Code
vhdl
sci01 RT-Code
vhdl
sv RT-Code
vhdl
vhdl+vlg
ncsim RT-Code
vhdl
vhdl+vlg
VHDL
Register-Transfer
VHDL
Gatternetzliste
Mixed-Mode
Simulator
Abstraktionsebene


32 x n-bit
5000
4500
4000
3500
3000
2500
2000
1500
1000
500
[s] 0
vss RT-Code
vhdl
sci01 RT-Code
vhdl
sv RT-Code
vhdl
vhdl+vlg
ncsim RT-Code
vhdl
vhdl+vlg
VHDL
Register-Transfer
VHDL
Gatternetzliste
Mixed-Mode
Simulator
Abstraktionsebene


25000
20000
15000
10000
5000
[s] 0
vss RT-Code
vhdl
sci01 RT-Code
vhdl
sv RT-Code
vhdl
vhdl+vlg
ncsim RT-Code
vhdl
vhdl+vlg
VHDL
VHDL
Mixed-Mode
Simulator
Register-Transfer
Gatternetzliste
Abstraktionsebene


5000
4500
4000
3500
3000
2500
2000
1500
1000
500
[s] 0
vss RT-Code
vhdl
sci01 RT-Code
vhdl
sv RT-Code
vhdl
vhdl+vlg
ncsim RT-Code
vhdl
vhdl+vlg
VHDL
VHDL
Mixed-Mode
Simulator
Register-Transfer
Gatternetzliste
Abstraktionsebene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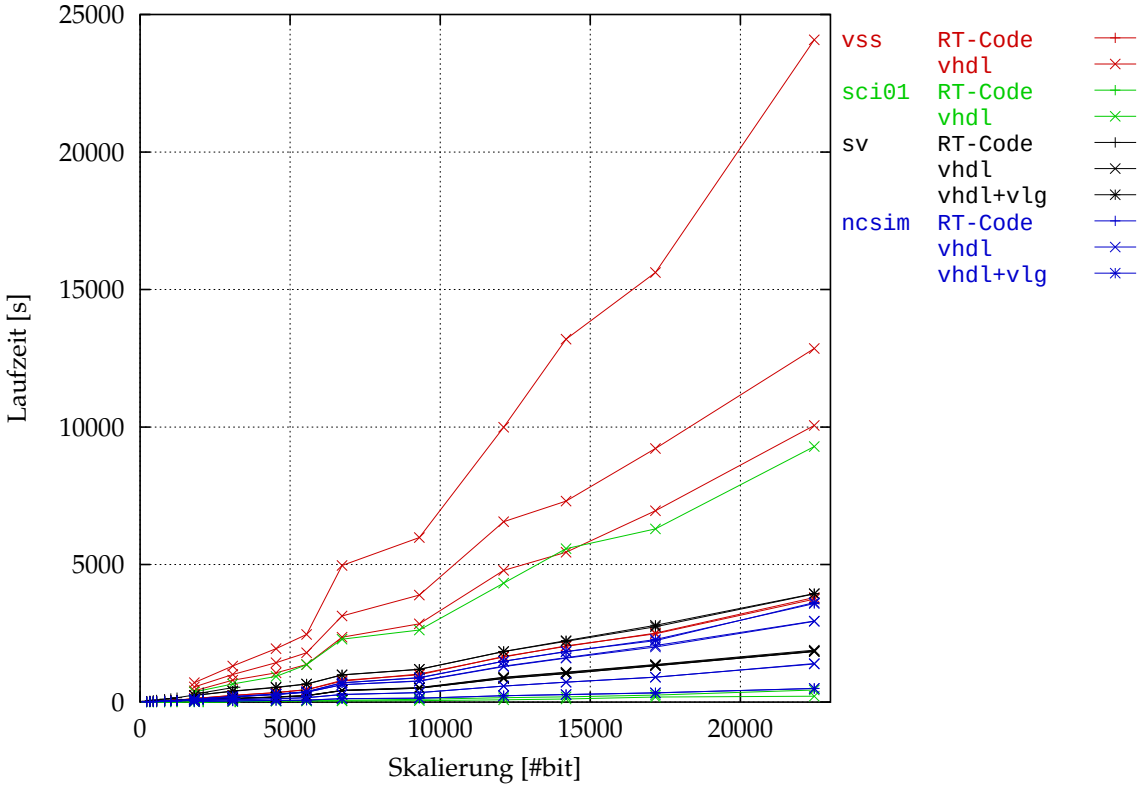
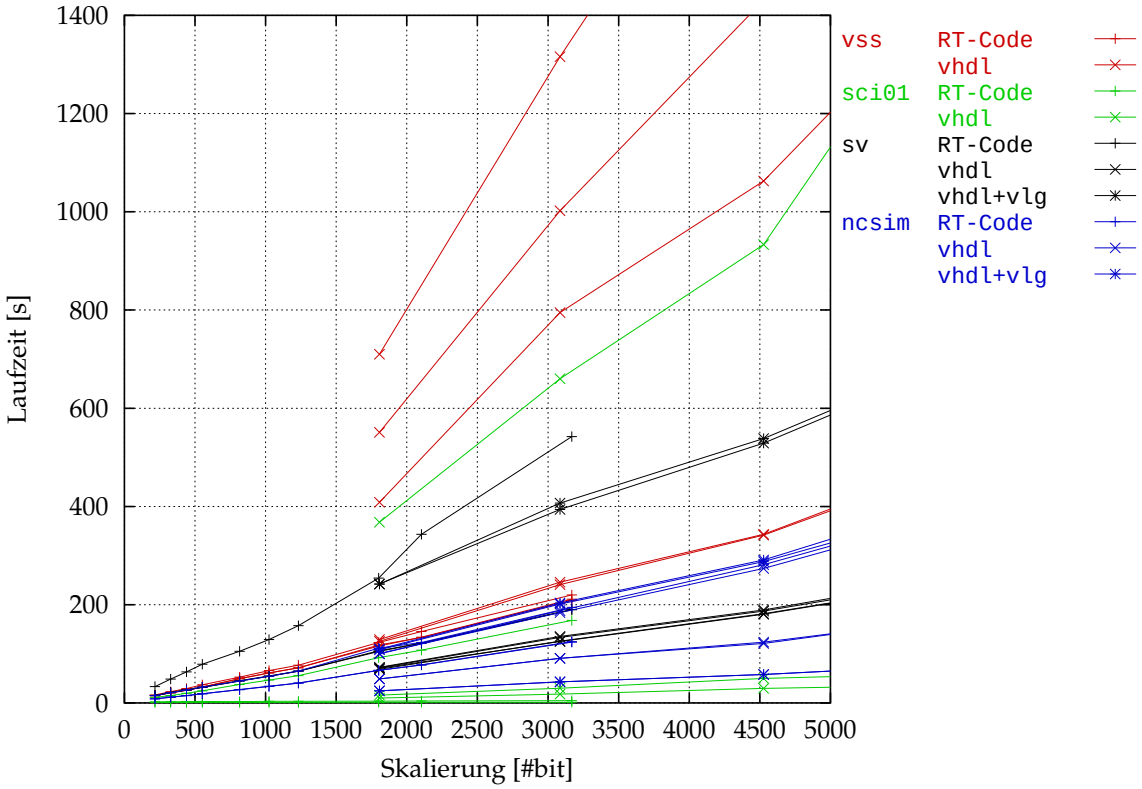
1600
1400
1200
1000
800
600
400
200
[s] 0
vss RT-Code
vhdl
sci01 RT-Code
vhdl
sv RT-Code
vhdl
vhdl+vlg
ncsim RT-Code
vhdl
vhdl+vlg
VHDL
VHDL
Mixed-Mode
Simulator
Register-Transfer
Gatternetzliste
Abstraktionsebene

3.6 Skalierung





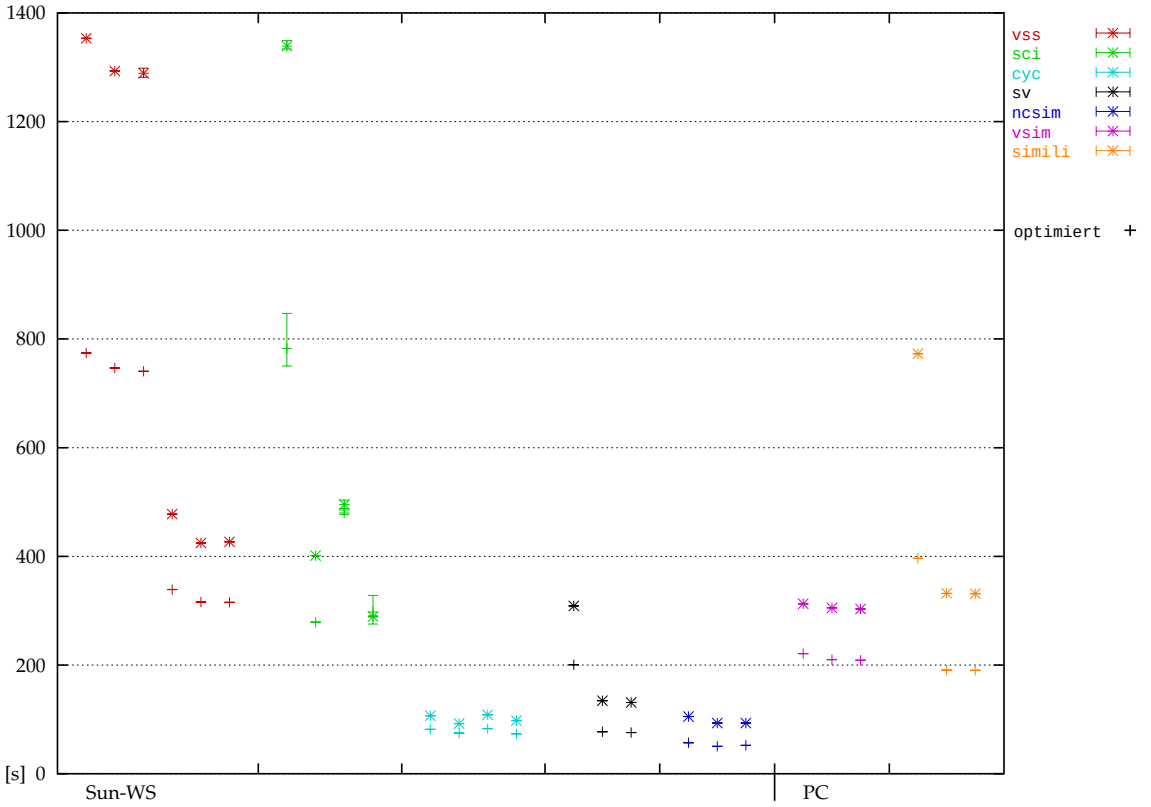
4 Fußgängerampel

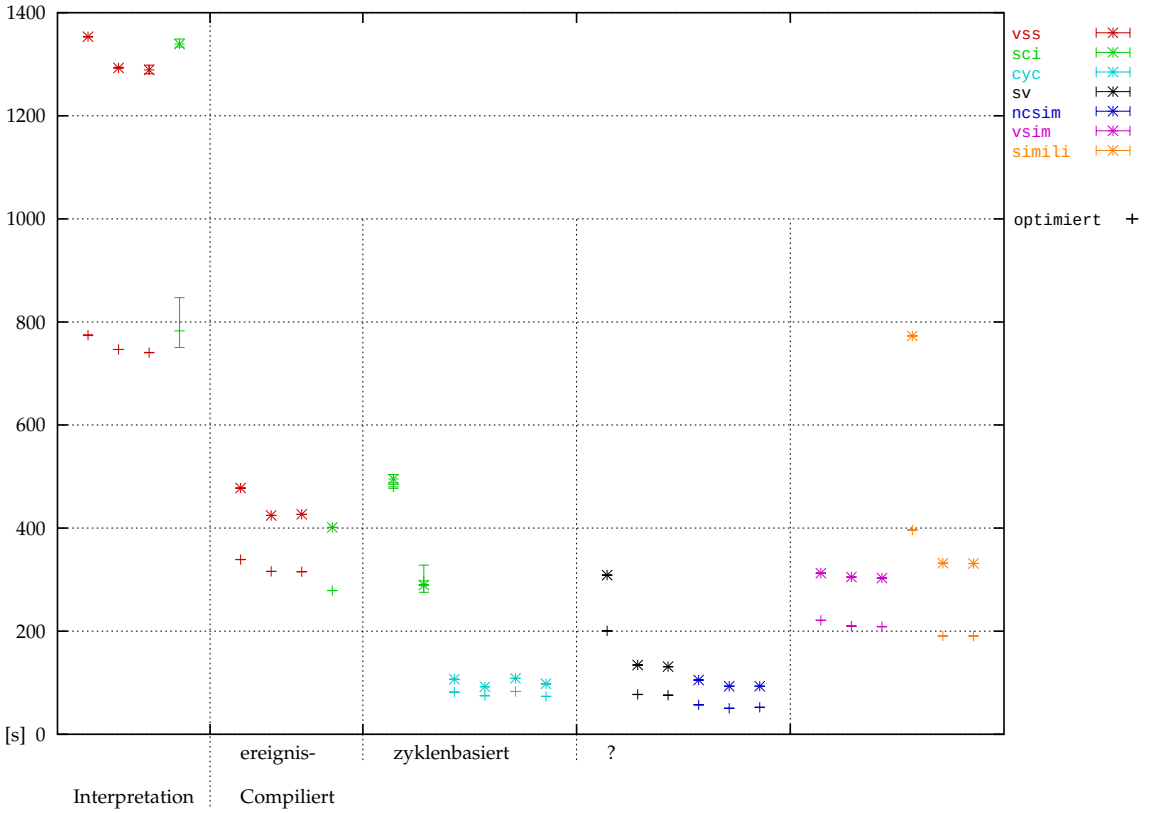
4.1 Register-Transfer Beschreibung

Tabelle 19: Fußgängerampel, RT-Code

Register-Transfer Code				
Simulator	4 Prozesse avg. $[s]$	1 Prozess avg. $[s]$	speed-up	Parameter
VSS	1353,29	774,38	1,75	vss.1
	1292,97	746,63	1,73	vss.2
	1288,92	740,62	1,74	vss.3
	477,68	339,02	1,41	vss.4
	424,59	316,02	1,34	vss.5
	426,68	315,43	1,35	vss.6
Scirocco	1339,06	782,76	1,71	sci.1
	401,41	278,88	1,44	sci.2
	495,27	479,92	1,03	sci.3
	289,33	297,6	0,98	sci.4
Cyclone	106,89	82,1	1,3	cyc.1
	92,2	74,82	1,23	cyc.2
	108,13	83,02	1,3	cyc.3
	96,5	73,93	1,31	cyc.4
Leapfrog	308,79	200,54	1,54	lea.1
	134,37	77,24	1,74	lea.2
	131,13	75,79	1,73	lea.3
NCSim	105,33	57,09	1,84	ncs.1
	93,28	50,4	1,85	ncs.2
	93,26	52,22	1,79	ncs.3
ModelSim	312,64	221,05	1,41	mod.1
	305,09	210,02	1,45	mod.2
	303,15	208,82	1,45	mod.3
Simili	772,88	396,34	1,95	sim.1
	331,82	190,72	1,74	sim.2
	331,36	190,46	1,74	sim.3

Fußgängerampel

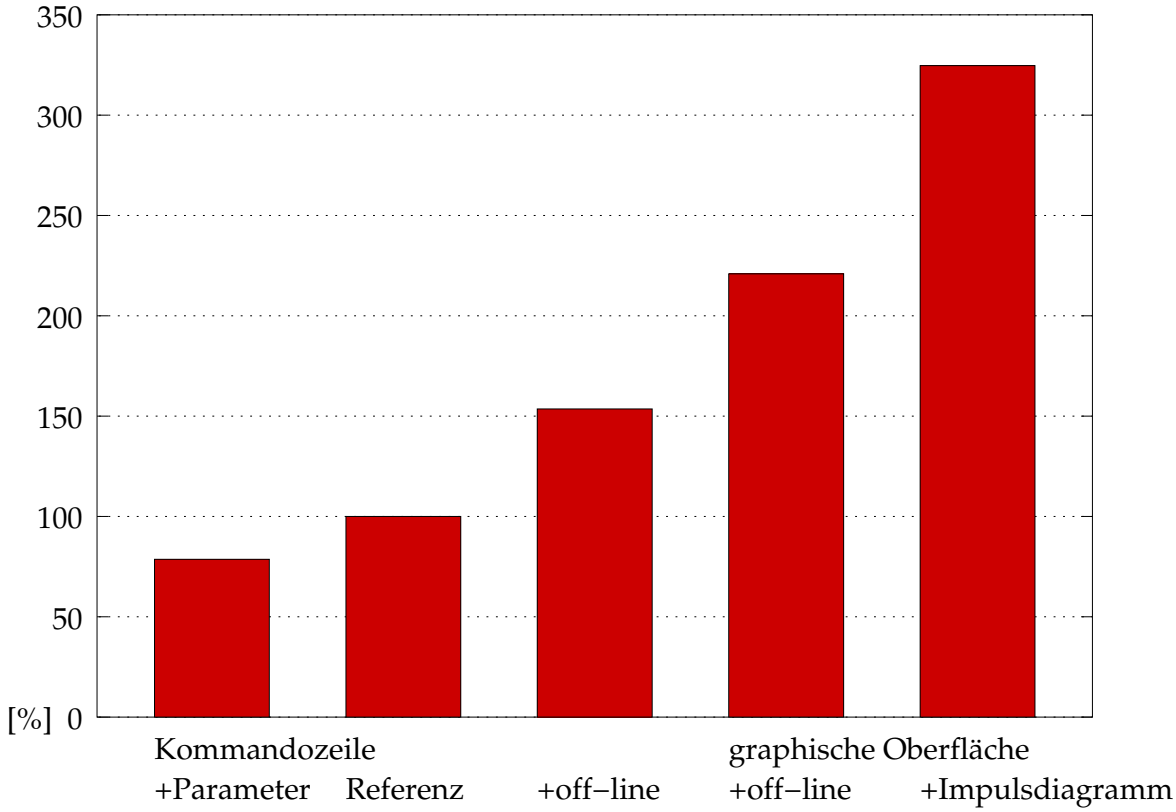




4.2 Benutzerinterface

Tabelle 20: Fußgängerampel, Benutzerschnittstelle

Benutzerschnittstelle		relative Geschwindigkeit
Kommandozeile	+Optimierungen bei Aufruf	78,66
–"–	Referenz	100,00
–"–	+off-line Signalauswertung	165,56
graphische Oberfläche	–"–	220,92
–"–	+Impulsdiagramm	324,69



5 Parametersätze

5.1 Simulationsprogramme

Tabelle 21: Programmparameter

Kommandozeilenparameter		
vss	v2000.12, bzw. 2001.09	WS
1	vhdlan -cycle -event ⟨*vhdFile*⟩ vhdlsim [-gfile ⟨*genFile*⟩] -d4 -fi_all -i ⟨*script*⟩ ⟨*config*⟩	
2	vhdlan -cycle -event ⟨*vhdFile*⟩ vhdlsim [-gfile ⟨*genFile*⟩] -d1 -fi_all -i ⟨*script*⟩ ⟨*config*⟩	
3	vhdlan -cycle -event ⟨*vhdFile*⟩ vhdlsim [-gfile ⟨*genFile*⟩] -fi_all -i ⟨*script*⟩ ⟨*config*⟩	
4	vhdlan -cycle -event ⟨*vhdFile*⟩ vhdlsim [-gfile ⟨*genFile*⟩] -d4 -i ⟨*script*⟩ ⟨*config*⟩	
5	vhdlan -cycle -event ⟨*vhdFile*⟩ vhdlsim [-gfile ⟨*genFile*⟩] -d1 -i ⟨*script*⟩ ⟨*config*⟩	
6	vhdlan -cycle -event ⟨*vhdFile*⟩ vhdlsim [-gfile ⟨*genFile*⟩] -i ⟨*script*⟩ ⟨*config*⟩	
sci	v2000.12	WS
1	vhdlan -cycle -event ⟨*vhdFile*⟩ scsim -time ⟨*unit*⟩ [-generics_file ⟨*genFile*⟩] -debug_all -include ⟨*script*⟩ ⟨*config*⟩	
2	vhdlan -cycle -event ⟨*vhdFile*⟩ scsim -time ⟨*unit*⟩ [-generics_file ⟨*genFile*⟩] -event_all -include ⟨*script*⟩ ⟨*config*⟩	
3	vhdlan -cycle -event ⟨*vhdFile*⟩ scsim -time ⟨*unit*⟩ [-generics_file ⟨*genFile*⟩] -partition ⟨*level1*⟩ -include ⟨*script*⟩ ⟨*config*⟩	
4	vhdlan -cycle -event ⟨*vhdFile*⟩ scsim -time ⟨*unit*⟩ [-generics_file ⟨*genFile*⟩] -partition ⟨*level0*⟩ -include ⟨*script*⟩ ⟨*config*⟩	
scm	v2000.12	WS
1	vhdlan -cycle -event ⟨*vhdFile*⟩ scsim -verilogcomp "-v ⟨*libFile*⟩ +cli ⟨*level1File*⟩" -time ⟨*unit*⟩ [-generics_file ⟨*genFile*⟩] -event_all -include ⟨*script*⟩ ⟨*config*⟩	
2	vhdlan -cycle -event ⟨*vhdFile*⟩ scsim -verilogcomp "-v ⟨*libFile*⟩ ⟨*level1File*⟩" -time ⟨*unit*⟩ [-generics_file ⟨*genFile*⟩] -event_all -include ⟨*script*⟩ ⟨*config*⟩	
3	vhdlan -cycle -event ⟨*vhdFile*⟩ scsim -verilogcomp "-v ⟨*libFile*⟩ +rad+2 ⟨*level1File*⟩" -time ⟨*unit*⟩ [-generics_file ⟨*genFile*⟩] -event_all -include ⟨*script*⟩ ⟨*config*⟩	
4	vhdlan -cycle -event ⟨*vhdFile*⟩ scsim -verilogcomp "-v ⟨*libFile*⟩ +cli +nospecify +notimingcheck ⟨*level1File*⟩" -time ⟨*unit*⟩ [-generics_file ⟨*genFile*⟩] -event_all -include ⟨*script*⟩ ⟨*config*⟩	
5	vhdlan -cycle -event ⟨*vhdFile*⟩ scsim -verilogcomp "-v ⟨*libFile*⟩ +nospecify +notimingcheck ⟨*level1File*⟩" -time ⟨*unit*⟩ [-generics_file ⟨*genFile*⟩] -event_all -include ⟨*script*⟩ ⟨*config*⟩	

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Kommandozeilenparameter			
	6	vhdlan -cycle -event ⟨*vhdFile*⟩ scsim -verilogcomp "-v ⟨*libFile*⟩ +rad+2 +nospecify +notimingcheck ⟨*level1File*⟩" -time ⟨*unit*⟩ [-generics_file ⟨*genFile*⟩] -event_all -include ⟨*script*⟩ ⟨*config*⟩	
scs		v2001.10, bzw. 2002.06	WS
	1	vhdlan -cycle -event ⟨*vhdFile*⟩ scs -time ⟨*unit*⟩ [-generics ⟨*genFile*⟩] -noperf ⟨*config*⟩ scsim -debug_all -include ⟨*script*⟩	
	2	vhdlan -cycle -event ⟨*vhdFile*⟩ scs -time ⟨*unit*⟩ [-generics ⟨*genFile*⟩] ⟨*config*⟩ scsim -include ⟨*script*⟩	
	3	vhdlan -cycle -event ⟨*vhdFile*⟩ scs -time ⟨*unit*⟩ [-generics ⟨*genFile*⟩] -partition ⟨*level1*⟩ ⟨*config*⟩ scsim -include ⟨*script*⟩	
	4	vhdlan -cycle -event ⟨*vhdFile*⟩ scs -time ⟨*unit*⟩ [-generics ⟨*genFile*⟩] -2state -partition ⟨*level0*⟩ ⟨*config*⟩ scsim -include ⟨*script*⟩	
scm		2002.06	WS
	1	vlogan [-y ⟨*libDir*⟩] {-v ⟨*libFile*⟩} ⟨*level1File*⟩ vhdlan -cycle -event ⟨*vhdFile*⟩ scs -verilogcomp "+cli" -time ⟨*unit*⟩ [-generics ⟨*genFile*⟩] ⟨*config*⟩ scsim -include ⟨*script*⟩	
	2	vlogan [-y ⟨*libDir*⟩] {-v ⟨*libFile*⟩} ⟨*level1File*⟩ vhdlan -cycle -event ⟨*vhdFile*⟩ scs -verilogcomp " " -time ⟨*unit*⟩ [-generics ⟨*genFile*⟩] ⟨*config*⟩ scsim -include ⟨*script*⟩	
	3	vlogan [-y ⟨*libDir*⟩] {-v ⟨*libFile*⟩} ⟨*level1File*⟩ vhdlan -cycle -event ⟨*vhdFile*⟩ scs -verilogcomp "+rad+2" -time ⟨*unit*⟩ [-generics ⟨*genFile*⟩] ⟨*config*⟩ scsim -include ⟨*script*⟩	
	4	vlogan [-y ⟨*libDir*⟩] {-v ⟨*libFile*⟩} +nospecify +notimingchecks ⟨*level1File*⟩ vhdlan -cycle -event ⟨*vhdFile*⟩ scs -verilogcomp "+cli +nospecify +notimingchecks" -time ⟨*unit*⟩ [-generics ⟨*genFile*⟩] ⟨*config*⟩ scsim -include ⟨*script*⟩	
	5	vlogan [-y ⟨*libDir*⟩] {-v ⟨*libFile*⟩} +nospecify +notimingchecks ⟨*level1File*⟩ vhdlan -cycle -event ⟨*vhdFile*⟩ scs -verilogcomp "+nospecify +notimingchecks" -time ⟨*unit*⟩ [-generics ⟨*genFile*⟩] ⟨*config*⟩ scsim -include ⟨*script*⟩	
	6	vlogan [-y ⟨*libDir*⟩] {-v ⟨*libFile*⟩} +nospecify +notimingchecks ⟨*level1File*⟩ vhdlan -cycle -event ⟨*vhdFile*⟩ scs -verilogcomp "+rad+2 +nospecify +notimingchecks" -time ⟨*unit*⟩ [-generics ⟨*genFile*⟩] ⟨*config*⟩ scsim -include ⟨*script*⟩	

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Kommandozeilenparameter			
cyc		v2000.12, bzw. 2001.09	WS
	1	vhdlan -cycle -event ⟨*vhdFile*⟩	
		cylab -t ⟨*unit*⟩ -4state -debug [-tbl] ⟨*config*⟩	
		cysim -t ⟨*unit*⟩ -4state -debug [-rewind] -i ⟨*script*⟩ ⟨*config*⟩	
	2	vhdlan -cycle -event ⟨*vhdFile*⟩	
		cylab -t ⟨*unit*⟩ -4state -perf [-tbl] ⟨*config*⟩	
		cysim -t ⟨*unit*⟩ -4state -perf [-rewind] -i ⟨*script*⟩ ⟨*config*⟩	
	3	vhdlan -cycle -event ⟨*vhdFile*⟩	
		cylab -t ⟨*unit*⟩ -2state -debug [-tbl] ⟨*config*⟩	
		cysim -t ⟨*unit*⟩ -2state -debug [-rewind] -i ⟨*script*⟩ ⟨*config*⟩	
	4	vhdlan -cycle -event ⟨*vhdFile*⟩	
		cylab -t ⟨*unit*⟩ -2state -perf [-tbl] ⟨*config*⟩	
		cysim -t ⟨*unit*⟩ -2state -perf [-rewind] -i ⟨*script*⟩ ⟨*config*⟩	
lea		v2.84-p001	WS
	1	cv -v93 -nobuiltin -noopt -nortl -novitalaccl ⟨*vhdFile*⟩	
		ev -v93 {-generic '⟨*genMap*⟩'} -preserve ⟨*config*⟩	
		sv -batch -input ⟨*script*⟩ ⟨*config*⟩	
	2	cv -v93 -avopt -performance ⟨*vhdFile*⟩	
		ev -v93 {-generic '⟨*genMap*⟩'} -performance ⟨*config*⟩	
		sv -batch -input ⟨*script*⟩ ⟨*config*⟩	
	3	cv -v93 -avopt -performance -bounds -underover -notcheck -vitalmsgoff -vitalxoff ⟨*vhdFile*⟩	
		ev -v93 {-generic '⟨*genMap*⟩'} -performance -noipd -notcheck -vitalmsgoff -vitalxoff ⟨*config*⟩	
		sv -batch -input ⟨*script*⟩ ⟨*config*⟩	
lem		v2.84-p001	WS
	1	VXLOPTS -v ⟨*libFile*⟩ -q -a	
		cv -v93 -avopt -performance ⟨*vhdFile*⟩	
		ev -v93 {-generic '⟨*genMap*⟩'} -performance ⟨*config*⟩	
		sv -batch -input ⟨*script*⟩ ⟨*config*⟩	
	2	VXLOPTS -v ⟨*libFile*⟩ -q -a +notimingchecks +turbo+3 +twin_turbo	
		cv -v93 -avopt -performance -bounds -underover -notcheck -vitalmsgoff -vitalxoff ⟨*vhdFile*⟩	
		ev -v93 {-generic '⟨*genMap*⟩'} -performance -noipd -notcheck -vitalmsgoff -vitalxoff ⟨*config*⟩	
		sv -batch -input ⟨*script*⟩ ⟨*config*⟩	
ncs		v3.11.(p1)	WS
	1	ncvhdl -v93 -nostdout -nolog -linedebug -nobuiltin ⟨*vhdFile*⟩	
		ncelab -v93 -nostdout -nolog {-generic '⟨*genMap*⟩'} -novitalaccl -ntc_warn ⟨*config*⟩	
		ncsim -batch -input ⟨*script*⟩ -nostdout -nokey ⟨*config*⟩	
	2	ncvhdl -v93 -nostdout -nolog ⟨*vhdFile*⟩	
		ncelab -v93 -nostdout -nolog {-generic '⟨*genMap*⟩'} ⟨*config*⟩	
		ncsim -batch -input ⟨*script*⟩ -nostdout -nokey ⟨*config*⟩	
	3	ncvhdl -v93 -nostdout -nolog -neverwarn -nopragmawarn -novitalcheck ⟨*vhdFile*⟩	
		ncelab -v93 -nostdout -nolog {-generic '⟨*genMap*⟩'} -neverwarn -notimingchecks -noipd -no_tchk_msg -no_tchk_xgen -no_vpd_msg -no_vpd_xgen ⟨*config*⟩	
		ncsim -batch -input ⟨*script*⟩ -nostdout -nokey -neverwarn -nocifcheck ⟨*config*⟩	

nächste Seite

Kommandozeilenparameter			
	4	ncvhdl	-v93 -nostdout -nolog -neverwarn -nopragmawarn -novitalcheck ⟨*vhdFile*⟩
		ncelab	-v93 -nostdout -nolog {-generic '⟨*genMap*⟩'} -noipd -no_tchk_msg -no_tchk_xgen -no_vpd_msg -no_vpd_xgen ⟨*config*⟩
		ncsim	-batch -input ⟨*script*⟩ -nostdout -nokey ⟨*config*⟩
	5	ncvhdl	-v93 -nostdout -nolog -neverwarn -nopragmawarn -novitalcheck ⟨*vhdFile*⟩
		ncelab	-v93 -nostdout -nolog {-generic '⟨*genMap*⟩'} -neverwarn -notimingchecks -noipd ⟨*config*⟩
		ncsim	-batch -input ⟨*script*⟩ -nostdout -nokey -neverwarn -nocifcheck ⟨*config*⟩
ncm		v3.11.(p1)	WS
	1	ncvlog	-nostdout -nolog ⟨*level1File*⟩
		ncvhdl	-v93 -nostdout -nolog ⟨*vhdFile*⟩
		ncelab	-v93 -nostdout -nolog {-generic '⟨*genMap*⟩'} ⟨*config*⟩
		ncsim	-batch -input ⟨*script*⟩ -nostdout -nokey ⟨*config*⟩
	2	ncvlog	-nostdout -nolog -neverwarn -nopragmawarn ⟨*level1File*⟩
		ncvhdl	-v93 -nostdout -nolog -neverwarn -nopragmawarn ⟨*vhdFile*⟩
		ncelab	-v93 -nostdout -nolog {-generic '⟨*genMap*⟩'} -neverwarn -notimingchecks -noipd -no_tchk_msg -no_tchk_xgen -no_vpd_msg -no_vpd_xgen ⟨*config*⟩
		ncsim	-batch -input ⟨*script*⟩ -nostdout -nokey -neverwarn -nocifcheck ⟨*config*⟩
ncv		v3.11.(p1)	WS
	1	ncvlog	-nostdout -nolog ⟨*vFile*⟩
		ncelab	-nostdout -nolog [-timescale ⟨*tScale*⟩] -access +R ⟨*module*⟩
		ncsim	-batch -input ⟨*script*⟩ -nostdout -nokey ⟨*module*⟩
	2	ncvlog	-nostdout -nolog ⟨*vFile*⟩
		ncelab	-nostdout -nolog [-timescale ⟨*tScale*⟩] [-afile ⟨*aFile*⟩] ⟨*module*⟩
		ncsim	-batch -input ⟨*script*⟩ -nostdout -nokey ⟨*module*⟩
	3	ncvlog	-nostdout -nolog -neverwarn -nopragmawarn ⟨*vFile*⟩
		ncelab	-nostdout -nolog [-timescale ⟨*tScale*⟩] [-afile ⟨*aFile*⟩] -neverwarn -notimingchecks -no_tchk_msg ⟨*module*⟩
		ncsim	-batch -input ⟨*script*⟩ -nostdout -nokey -neverwarn -epulse_no_msg -plinowarn ⟨*module*⟩
mod		v5.3d	PC
	1	vcom	-93 -no1164 -novital -noaccel numeric_std -O0 ⟨*vhdFile*⟩
		vsim	-c -do ⟨*script*⟩ ⟨*config*⟩
	2	vcom	-93 ⟨*vhdFile*⟩
		vsim	-c -do ⟨*script*⟩ ⟨*config*⟩
	3	vcom	-93 -nocheck -O5 ⟨*vhdFile*⟩
		vsim	-c -do ⟨*script*⟩ ⟨*config*⟩
sim		v1.5b17	PC
	1	vhdlp	⟨*vhdFile*⟩
		vhdle	[-t ⟨*simTime*⟩] -strict -noaccel ALL -nocycleopt ⟨*config*⟩
	2	vhdlp	⟨*vhdFile*⟩
		vhdle	[-t ⟨*simTime*⟩] ⟨*config*⟩
	3	vhdlp	⟨*vhdFile*⟩
		vhdle	[-t ⟨*simTime*⟩] -p -nowarn ALL ⟨*config*⟩

nächste Seite

Kommandozeilenparameter			
vcs	v6.0.1, bzw. v6.2R4		WS
1	`vcs`	`-q -k off [-y ⟨libDir⟩] {-v ⟨libFile⟩} ⟨vFile-List⟩`	
	`simv`	`-q`	
2	`vcs`	`-q -k off [-y ⟨libDir⟩] {-v ⟨libFile⟩} +rad+2 +delay_mode_zero +nospecify ⟨vFile-List⟩`	
	`simv`	`-q`	
3	`vcs`	`-q -k off [-y ⟨libDir⟩] {-v ⟨libFile⟩} +rad+2 +delay_mode_zero +nospecify +notimingcheck +no_notifier +no_tchk_msg ⟨vFile-List⟩`	
	`simv`	`-q`	
4	`vcs`	`-q [-y ⟨libDir⟩] {-v ⟨libFile⟩} +cli ⟨vFile-List⟩`	
	`simv`	`-q`	
5	`vcs`	`-q [-y ⟨libDir⟩] {-v ⟨libFile⟩} ⟨vFile-List⟩`	
	`simv`	`-q`	
6	`vcs`	`-q [-y ⟨libDir⟩] {-v ⟨libFile⟩} +rad+2 ⟨vFile-List⟩`	
	`simv`	`-q`	
7	`vcs`	`-q [-y ⟨libDir⟩] {-v ⟨libFile⟩} +cli +nospecify +notimingchecks ⟨vFile-List⟩`	
	`simv`	`-q`	
8	`vcs`	`-q [-y ⟨libDir⟩] {-v ⟨libFile⟩} +nospecify +notimingchecks ⟨vFile-List⟩`	
	`simv`	`-q`	
9	`vcs`	`-q [-y ⟨libDir⟩] {-v ⟨libFile⟩} +rad+2 +nospecify +notimingchecks ⟨vFile-List⟩`	
	`simv`	`-q`	
ver	v3.11.p001		WS
1	`verilog`	`-q [-y ⟨libDir⟩] {-v ⟨libFile⟩} ⟨vFile-List⟩`	
2	`verilog`	`-q [-y ⟨libDir⟩] {-v ⟨libFile⟩} +notimingchecks +turbo+3 +twin_turbo ⟨vFile-List⟩`	

	Maschine	Betriebssystem	Prozessor	Speicher
WS	Sun Ultra-60	Sun OS 5.8	2×360 MHz	1 280 MB
PC	PC, AMD K6-III	Windows ME	400 MHz	160 MB

5.2 Gatterbibliotheken

Tabelle 22: Gatterbibliotheken

Gatterbibliotheken		
VSS, Scirocco		
•	`vhdlan`	`-nocycle -event -optimize -work` ⟨*libId*⟩ ⟨*vhdLibFile*⟩
• FTGS	`lc_shell`	`> read_lib` ⟨*libSource*⟩
		`> vhdllib_architecture="FTGS"`
		`> write_lib -format vhdl` ⟨*libId*⟩
	`vhdlan`	`-nocycle -noevent -work` ⟨*libId*⟩ ⟨*vhdLibFile*⟩
• FTGSC	⟨*model*⟩ ::= FTGS|FTSM|UDSM|VITAL	
FTSM	`lc_shell`	`> read_lib` ⟨*libSource*⟩
UDSM		`> vhdllib_architecture="`⟨*model*⟩`"`
VITAL		`> write_lib -format vhdl` ⟨*libId*⟩
	`vhdlan`	`-nocycle -event -work` ⟨*libId*⟩ ⟨*vhdLibFile*⟩
• vital	`vhdlan`	`-nocycle -event -optimize -work` ⟨*libId*⟩ ⟨*vhdLibFile*⟩
Leapfrog		
•	`cv`	`-v93 -avopt -performance -work` ⟨*libId*⟩ ⟨*vhdLibFile*⟩
• opt	`cv`	`-v93 -avopt -performance -bounds -underover -notcheck`
		`-vitalmsgoff -vitalxoff -work` ⟨*libId*⟩ ⟨*vhdLibFile*⟩
NCSim		
• vhdl	`ncvhdl`	`-v93 -nostdout -nolog -work` ⟨*libId*⟩ ⟨*vhdLibFile*⟩
• vlog	`ncvlog`	`-nostdout -nolog -work` ⟨*libId*⟩ ⟨*vLibFile*⟩

5.3 Schaltungsgrößen

Tabelle 23: Größe der Benchmarkschaltungen

Fußgängerampel		Instanzen	Prozesse	Signale	Bit
Source	`tlcWalk(proc4)`		4	4	
	`tlcWalk(proc1)`		1		
	`tlcTst`	1	1	5	
RT-Code	4 Prozesse	1	5	9	12
	1 Prozess	1	2	5	8

Operationswerk		Instanzen	Prozesse	Signale	Bit
Source	`alu`		1		
	`opw`	1	6	12	
	`opwTst`	1	1	10	
RT-Code		2	8	22	272
Netzliste	AMS	779	3489	3610	3632
	UMC	823	3202	3179	3201

Funkwecker		Instanzen	Prozesse	Signale	Bit
Source	`clkGen`		7	3	
	`ctrlFsm`		4	6	
	`dcfFsm`		19	13	
	`alaFsm`		3	4	
	`alaBlk`		6	24	

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		Instanzen	Prozesse	Signale	Bit
	`timBlk`		2	1	
	`display`		2		
	`dcfClock`	7		53	
	`dcfSend`		2	1	
	`tstClock`	2	3	25	
RT-Code		9	48	130	405
Netzliste	AMS	1620	6472	6811	6876
	UMC	1726	6388	6502	6560

Booth-Multiplizierer		Instanzen	Prozesse	Signale	Bit
Source	`mul8`		13	12	
	`mul16`		25	24	
	`mul24`		37	36	
	`mul32`		49	48	
	`mulTst`	1	1	3	
RT-Code	`8× 8`	1	14	15	216
	`8×16`	1	14	15	328
	`8×24`	1	14	15	440
	`8×32`	1	14	15	552
	`16×16`	1	26	27	816
	`16×24`	1	26	27	1024
	`16×32`	1	26	27	1232
	`24×24`	1	38	39	1800
	`24×32`	1	38	39	2104
	`32×32`	1	50	51	3168
Netzliste	`8× 8`	603	1760	1762	1806
AMS	`8×16`	1039	3015	3017	3085
	`8×24`	1517	4433	4435	4527
	`8×32`	1830	5429	5431	5547
	`16×16`	2266	6636	6638	6730
	`16×24`	3109	9188	9190	9306
	`16×32`	4036	11971	11973	12113
	`24×24`	4707	14048	14050	14190
	`24×32`	5614	17003	17005	17169
	`32×32`	7359	22271	22273	22461