FPGA: Field-Programmable Gate-Array

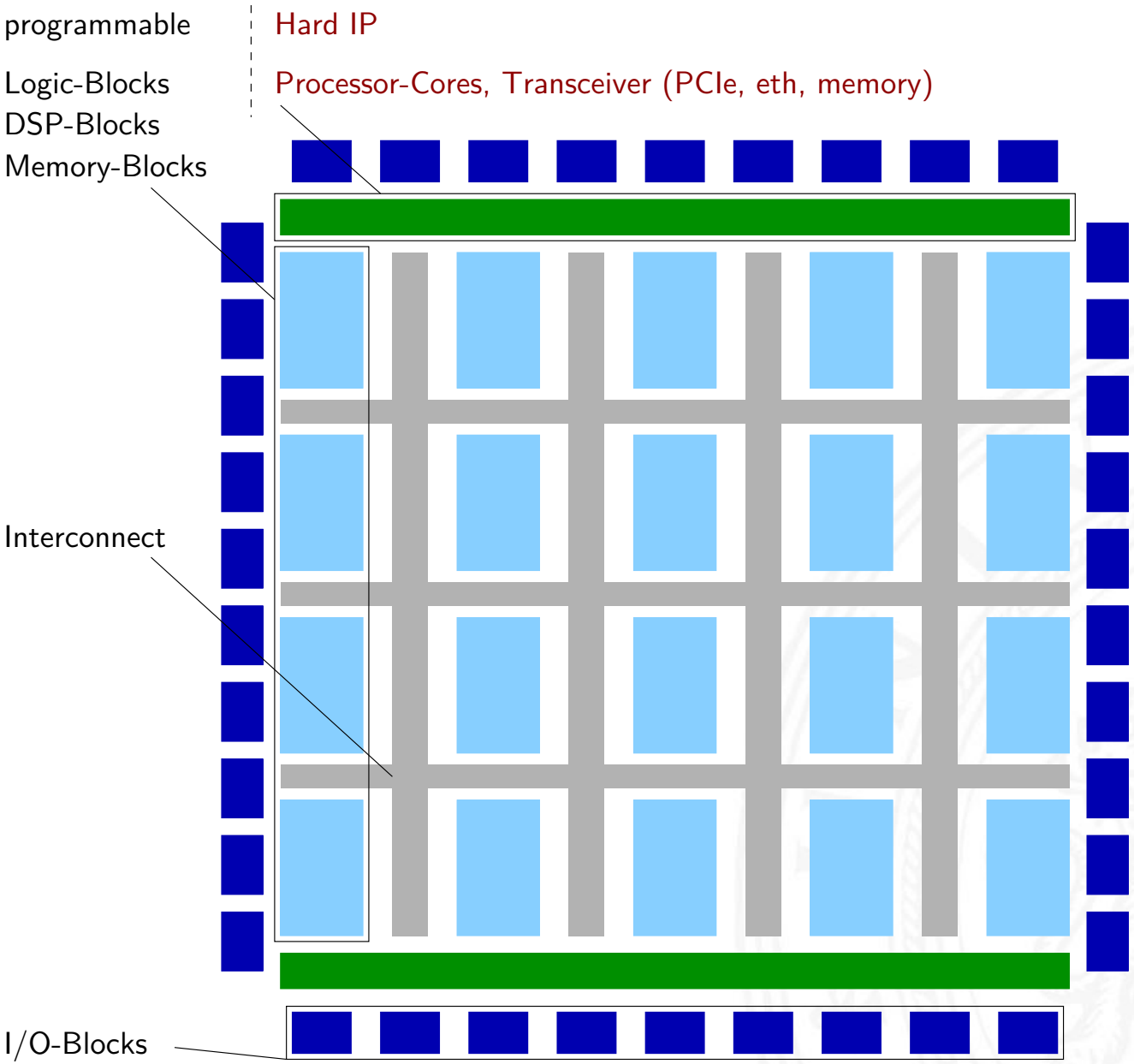
Sammelbegriff für „große“ anwenderprogrammierbare Schaltungen

- Matrix von kleineren programmierbaren Zellen, beispielsweise
  - SRAM als Lookup für Funktionen
  - programmierbare Register
  - Carry-Lookahead Logik
- Multiplexer-Netzwerk als programmierbare Verbindung
- zusätzliche „Makrozellen“
  - Multiplizierer, FP-Recheneinheiten, KI-Beschleuniger
  - eingebettete Prozessorkerne
  - A/D + D/A Wandler
- IO-Zellen
  - schnelle serielle Kommunikation
  - PLLs (programmierbare Taktgeneratoren)
- generierte Komponenten: ROM, RAM, FIFO ...

FPGA: Field-Programmable Gate-Array (cont.)

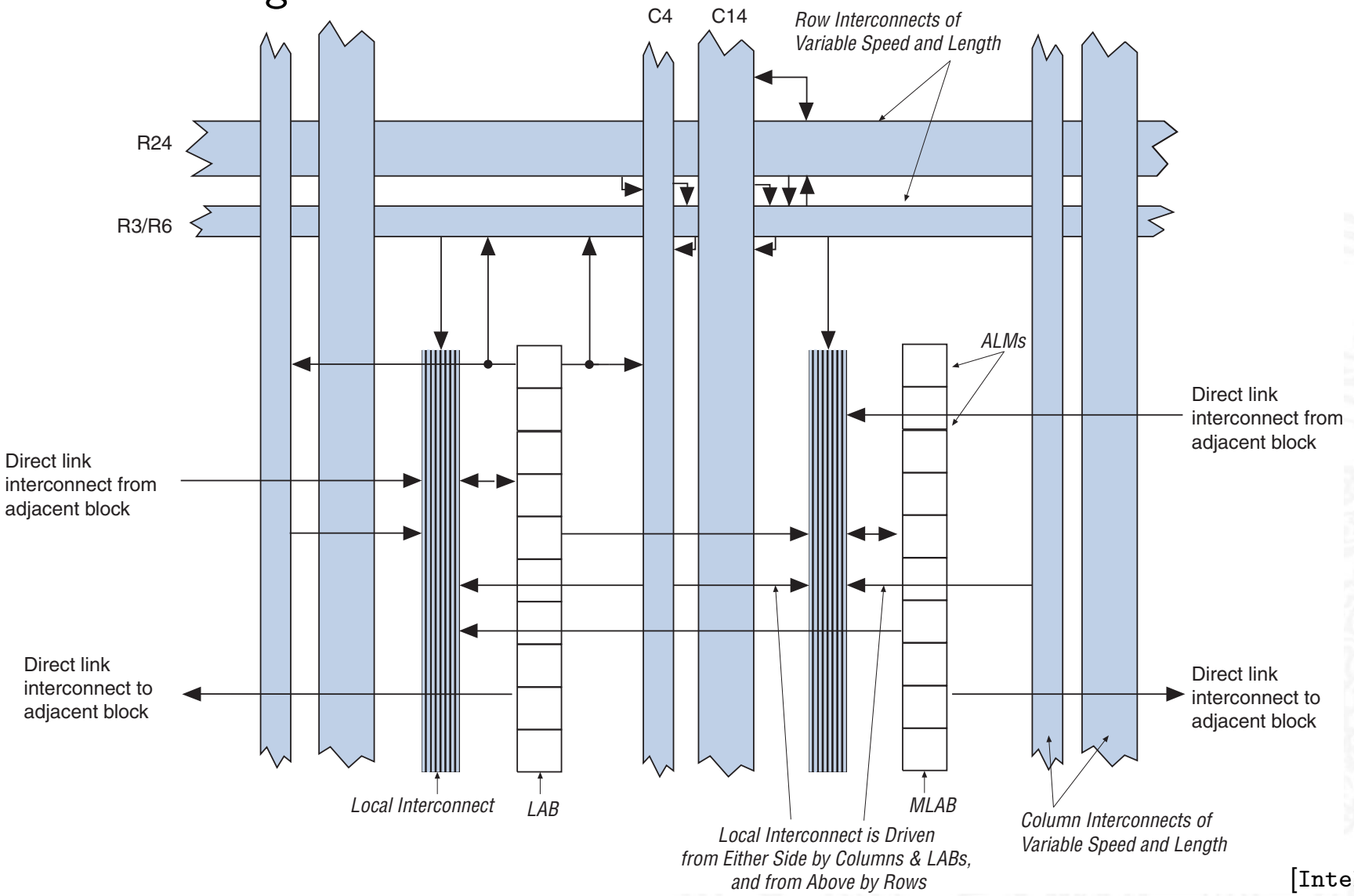
- fertige IP-Blöcke („*Intellectual Property*“), vergleichbar Bibliotheksfunktionen in Programmierung
  - Netzwerkprotokolle (Ethernet . . .)
  - Speichercontroller
  - Bussysteme (PCIe . . .)
  - . . .
- Komplexität
  - ≈ 3 000 nutzbare I/O
  - ≈ 40 Mio. Register (1-bit)
  - ≈ 2,0 GHz, 7 nm Prozesstechnik
  - ≈ 92 Mrd. Transistoren
- Hersteller
  - Xilinx Inc. (Advanced Micro Devices, Inc.),
  - Intel Corporation (ex. Altera),
  - Microchip Technology Inc.,
  - Lattice Semiconductor Corporation,
  - Achronix Semiconductor Corporation, . . .

Aufbau: programmierbare + fest vorgebene Bereiche



Aufbau: Beispiel

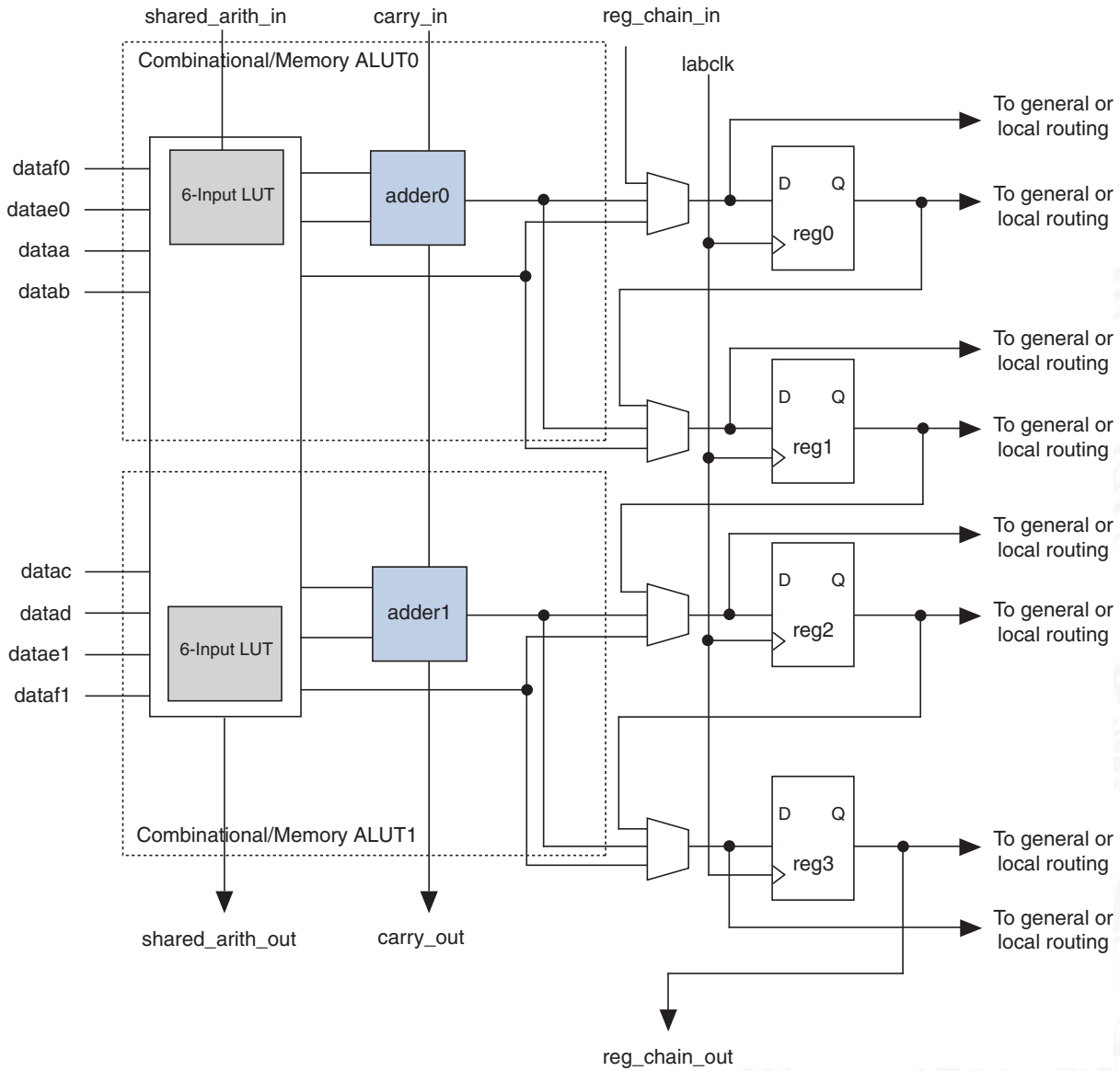
- Verbindungsnetzwerk



[IntelFPGA]

Aufbau: Beispiel (cont.)

- programmierbarer Block

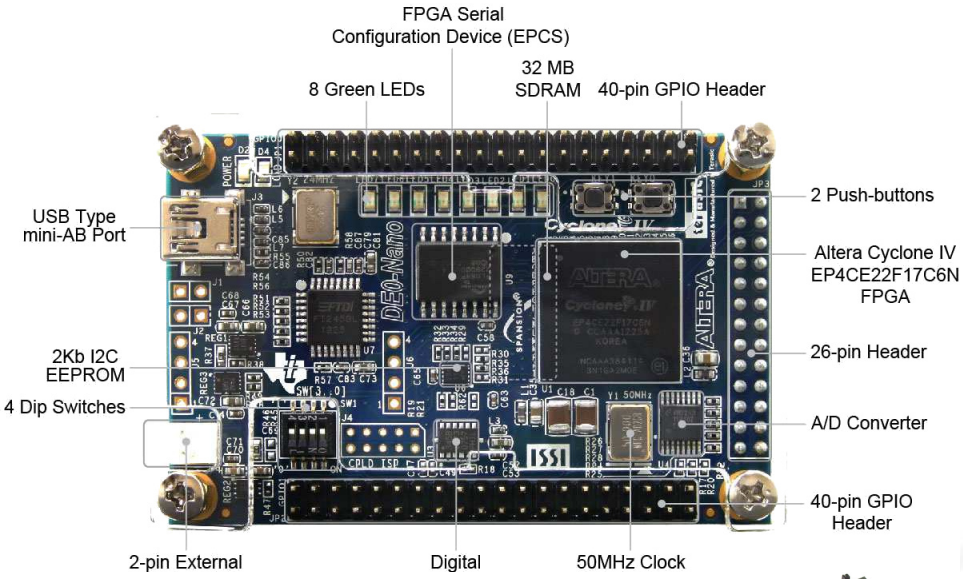


[IntelFPGA]

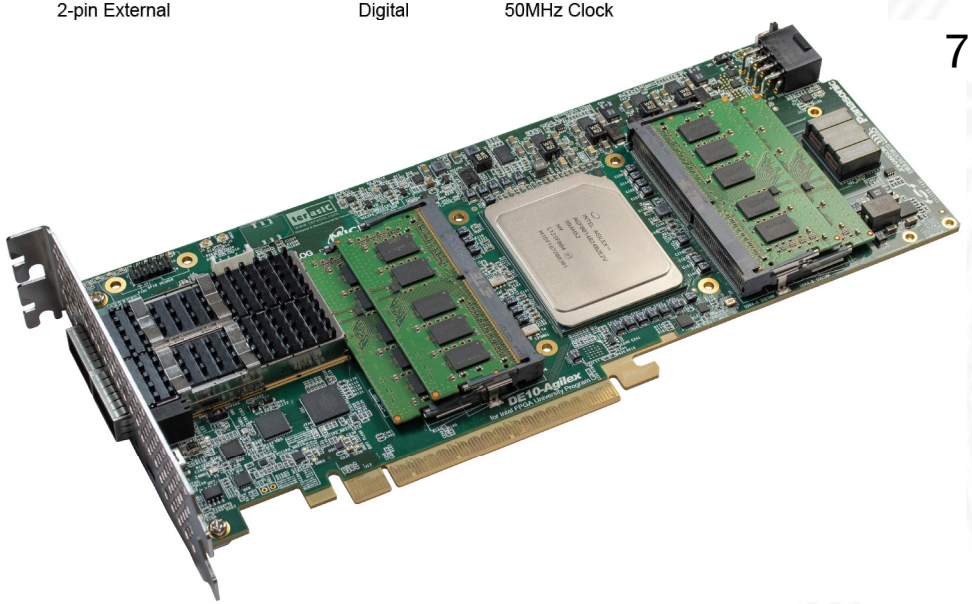
Aufbau: Beispiel (cont.)

- Prototypenplatinen

[TerasIC]



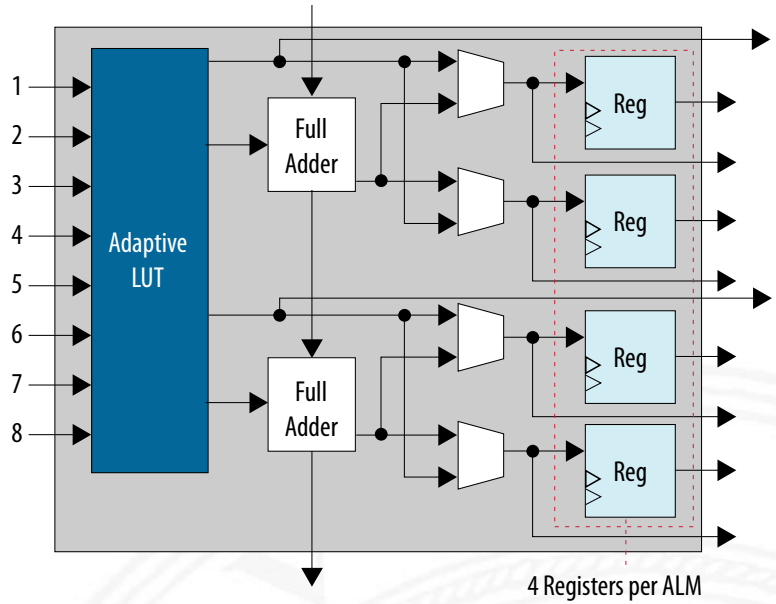
$< 100\,\$$



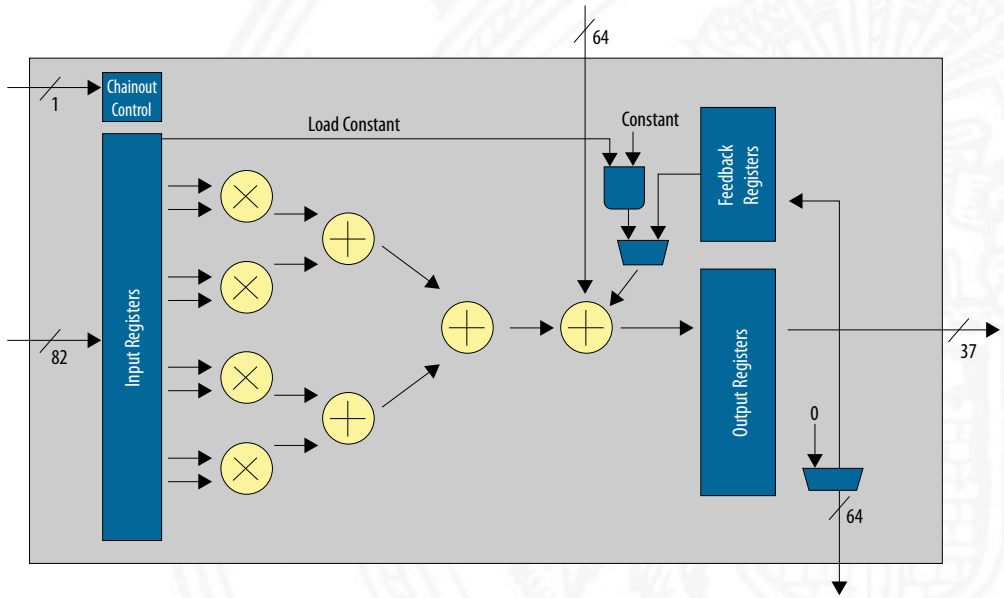
$7\,345\,\$$

Beispiel

- Logic-Block



- DSP-Block

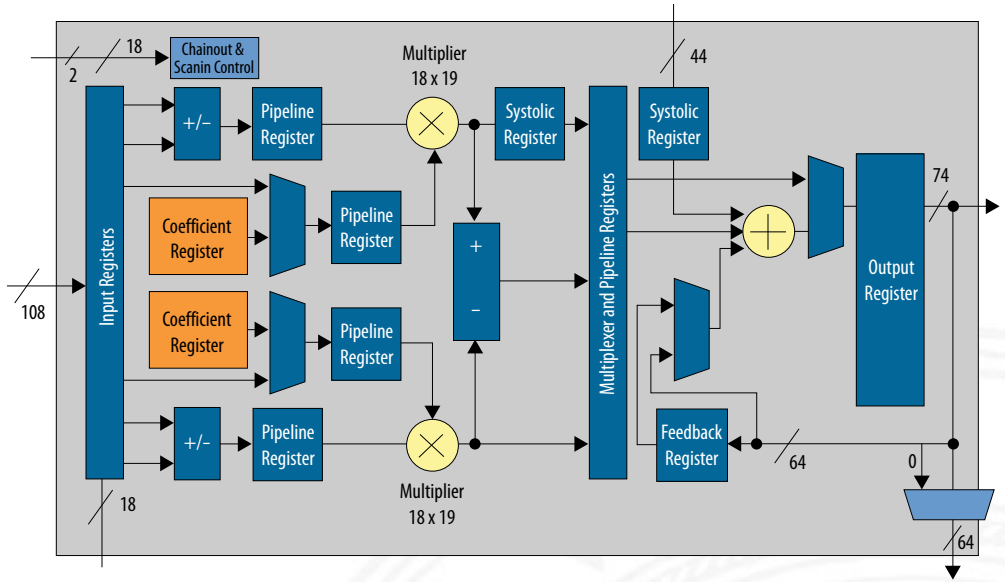


Intel Agilex FPGA Advanced Information Brief [Intel-Agilex]

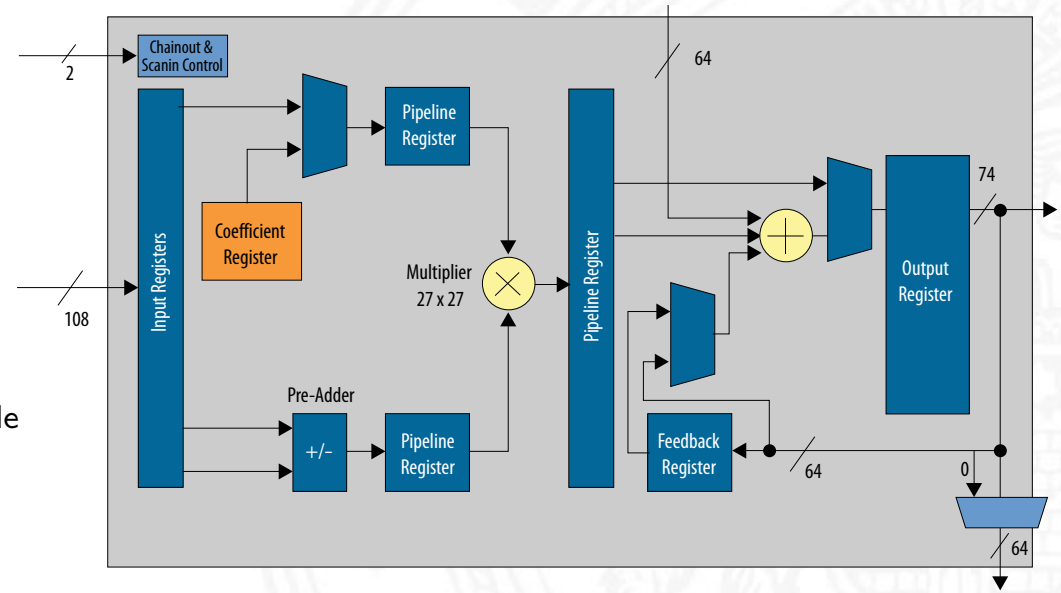
Beispiel (cont.)

- DSP-Block

Standard Precision Fixed Point Mode

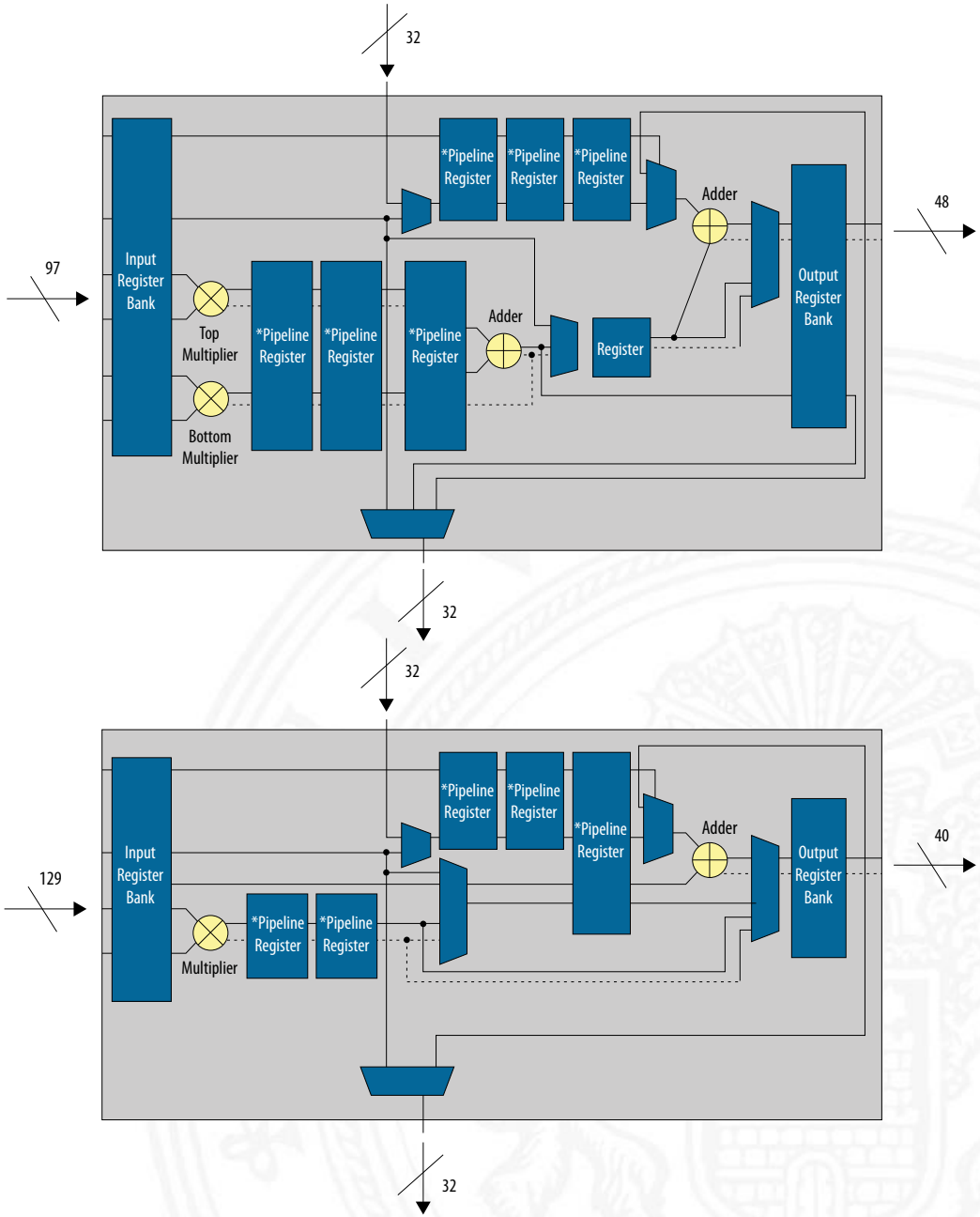


High Precision Fixed Point Mode



Beispiel (cont.)

- DSP-Block



Half Precision Floating Point (16-bit)

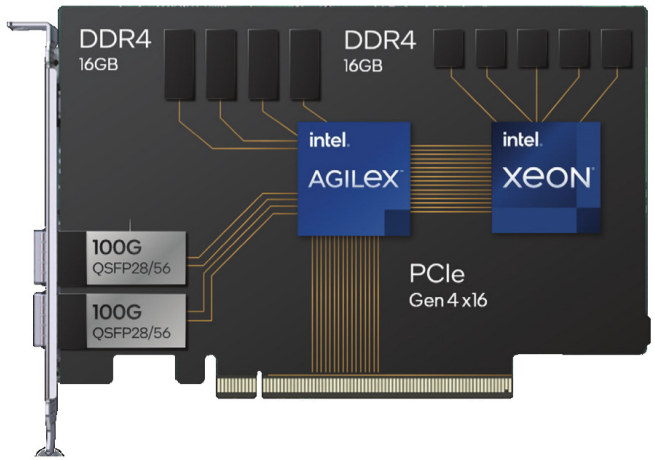
Single Precision Floating Point (32-bit)

FPGA Komplexität

Intel Agilex

[IntelFPGA]

Intel Agilex F-Series Device Names	Logic Elements (LE)	eSRAM Blocks	eSRAM Mbits	M20K Blocks	M20K Mbits	MLAB Counts	MLAB Mbits	Variable Precision DSP Blocks	18x19 Multipliers
AGF 004	392,000	0	0	1,900	38	6644	4.3	1,640	2.3K
AGF 006	573,480	0	0	2,844	56	9720	6.2	1,640	3.3K
AGF 008	764,640	0	0	3,792	74	12960	8.3	2,296	4.6K
AGF 012	1,200,000	2	36	5,568	110	20338	13	4,000	8K
AGF 014	1,437,240	2	36	7,110	139	24,360	15.6	4,510	9K
AGF 022	2,200,000	0	0	11,616	210	37288	21	6,250	12.5K
AGF 027	2,692,760	0	0	13,272	259	45,640	29.2	8,736	17K



FPGA Komplexität (cont.)

- Xilinx Versal [Xilinx]

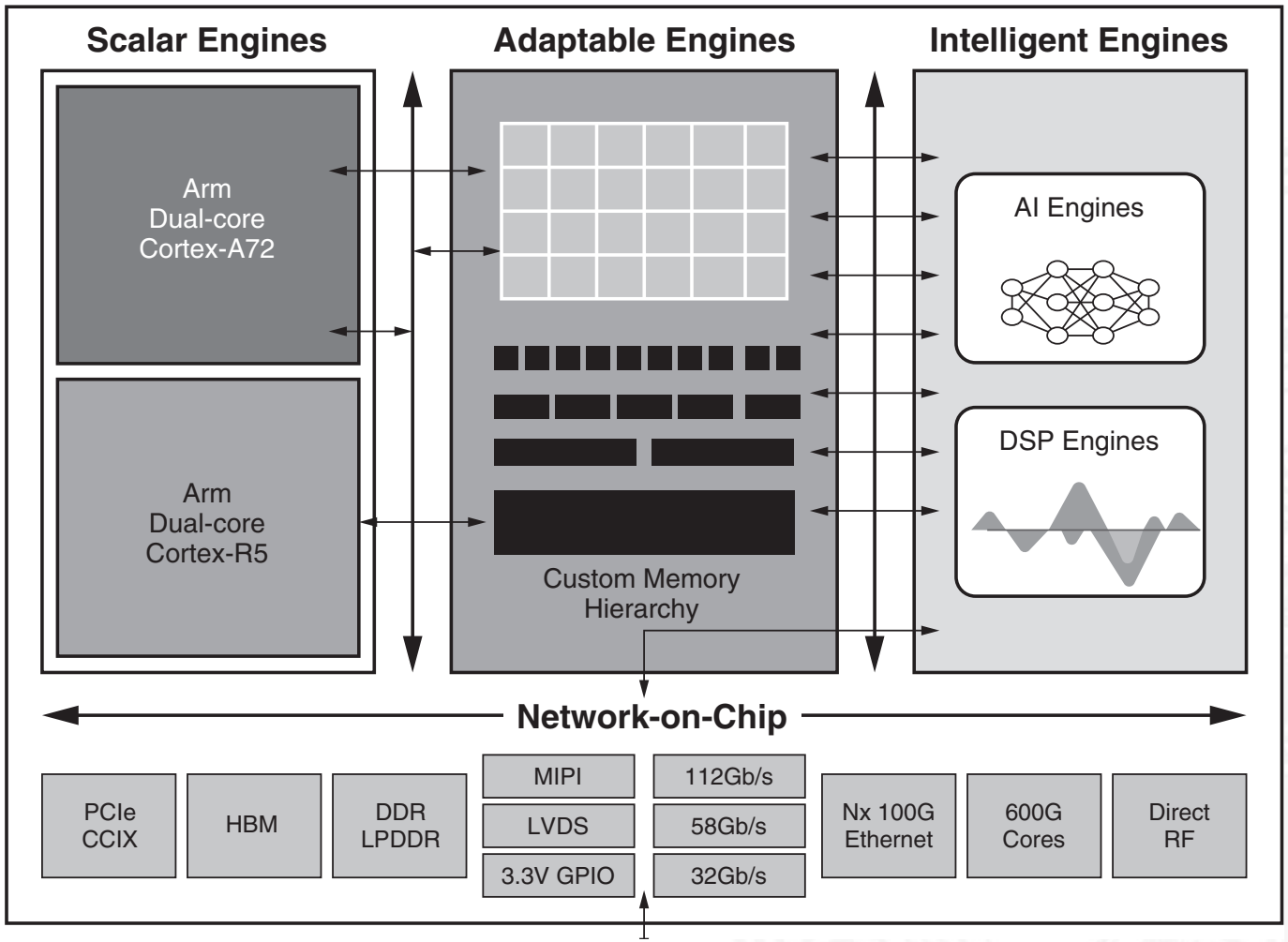
		VP1002	VP1052	VP1102	VP1202	VP1402	VP1502	VP2502	VP1552	VP1702	VP1802	VP2802
Adaptable Engines	System Logic Cells (K)	833	1,186	1,575	1,969	2,233	3,763	3,738	3,837	5,558	7,352	7,326
	LUTs	380,800	542,080	719,872	900,224	1,020,928	1,720,448	1,708,672	1,753,984	2,540,672	3,360,896	3,349,120
	NoC Master / NoC Slave Ports	22	22	30	28	42	52	52	52	76	100	100
	Distributed RAM (Mb)	12	17	22	27	31	53	52	54	78	103	102
Memory	Total Block RAM (Mb)	19	26	49	47	70	89	89	89	132	174	174
	UltraRAM (Mb)	97	138	127	190	181	366	366	366	541	717	717
	Total PL Memory (Mb)	128	181	198	264	282	508	507	509	751	994	994
	DDR Memory Controllers	2	2	3	4	3	4	4	4	4	4	4
	DDR Bus Width	128	128	192	256	192	256	256	256	256	256	256
Intelligent Engines	DSP Engines	1,140	1,572	1,904	3,984	2,672	7,440	7,392	7,392	10,896	14,352	14,304
	AI Engines Tiles	-	-	-	-	-	-	472	-	-	-	472
	AI Engine Data Memory (Mb)	-	-	-	-	-	-	118	-	-	-	118
Scalar Engines	APU	Dual-core Arm® Cortex®-A72, 48KB/32KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC										
	RPU	Dual-core Arm Cortex-R5F, 32KB/32KB L1 Cache, and 256KB TCM w/ECC										
	Memory	256KB On-Chip Memory w/ECC										
	Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)										
Serial Transceivers	GTY Transceivers (32.75Gb/s)	20	20	-	-	-	-	-	-	-	-	-
	GTYP Transceivers (32.75Gb/s)	-	-	8	28(1)	8	28(1)	28(1)	68(1)	28(1)	28(1)	28(1)
	GTM Transceivers(2) (58G (112G))	24 (12)	48 (24)	64 (32)	20 (10)	96 (64)	60 (30)	60 (30)	20 (10)	100 (50)	140 (70)	140 (70)
Integrated Protocol IP	PCIe® w/DMA & CCIX (CPM4)	2 x Gen4x4	2 x Gen4x4	-	-	-	-	-	-	-	-	-
	PCIe w/DMA & CCIX (CPM5)	-	-	-	2 x Gen5x8	-	2 x Gen5x8	2 x Gen5x8	2 x Gen5x8	2 x Gen5x8	2 x Gen5x8	2 x Gen5x8
	PCI Express	1 x Gen4x8	1 x Gen4x8	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4	8 x Gen5x4	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4
	100G Multirate Ethernet MAC	3	5	6	2	6	4	4	4	6	8	8
	600G Ethernet MAC	2	3	7	1	11	3	3	1	5	7	7
	600G Interlaken	1	2	0	0	0	1	1	0	2	3	3
	400G High-Speed Crypto Engine	1	1	3	1	4	2	2	2	3	4	4
Ordering Information	Extended(3)	-1MSE, -1LSE, -2MSE, -2MLE, -2LSE, -2LLE		-1MSE, -1LSE, -2MSE, -2MLE, -2LSE, -2LLE, -3HSE								
	Industrial(3)	-1MSI, -1MLI, -1LSI, -1LLI, -2MSI, -2MLI, -2LLI, -2HSI		-1MSI, -1MLI, -1LSI, -1LLI, -2MSI, -2MLI								

⇒ FPGAs derzeit komplexeste ICs (≈ 92 Milliarden Transistoren)

2022: NVIDIA GH100 80 Mrd.

Zukunftskonzepte

- Rechenbeschleuniger in Workstations und PCs
- dynamische (Teil-) Konfiguration zur Programmlaufzeit



Xilinx Versal ACAP (Adaptive Compute Acceleration Platform) [Xilinx-Versal]